Regulations and Curriculum for

Master of Technology (M. Tech.)

in

VLSI Design and Embedded Systems

(Deemed to be University under Section 3 of UGC Act, 1956)

(Placed under Category 'A' by MHRD, Govt. of India, Accredited with 'A+' Grade by NAAC)

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REGULATIONS GOVERNING
THE DEGREE OF MASTER OF TECHNOLOGY (M.Tech.)

UNDER OUTCOME BASED EDUCATION (OBE)

AND

CHOICE BASED CREDIT SYSTEM (CBCS) SCHEME

OF

NMAM INSTITUTE OF TECHNOLOGY, NITTE

(Effective from academic year 2022 -23)

VISION

To build a humane society through excellence in the education and healthcare

MISSION

To develop Nitte (Deemed to be University)
As a centre of excellence imparting quality education, Generating competent, skilled manpower to face the scientific and social challenges with a high degree of credibility, integrity, ethical standards and social concern

NITTE (Deemed to be University) | NMAM INSTITUTE OF TECHNOLOGY

Off-campus Centre, Nitte (Deemed to be University)

NITTE-574110, Karkala Taluk, Udupi District, Karnataka, India

Vision Statement

Pursuing Excellence, Empowering people, Partnering in Community Development

Mission Statement

To develop N.M.A.M. Institute of Technology, Nitte, as Centre of Excellence by imparting Quality Education to generate Competent, Skilled and Humane Manpower to face emerging Scientific, Technological, Managerial and Social Challenges with Credibility, Integrity, Ethics and Social Concern.

M. Tech. Regulations and Curriculum

Batch

2022 – 2024

With Scheme of Teaching & Examination

REGULATIONS: 2022

for

M. Tech. Programs

(Academic year 2022-23)

COMMON TO ALL

M.Tech. DEGREE PROGRAMS

CHOICE BASED CREDIT SYSTEM (CBCS)

Key Information

Program Title	Master of Technology, abbreviated as **M.Tech. (VLSI Design and Embedded Systems)**
Short description	Two-year, four semester Choice Based Credit System (CBCS) type of Postgraduate Engineering Degree Program with English as medium of instruction
Program Code	22ENGR19D2
Revision version	2022.01 These regulations may be modified from time to time as mandated by the policies of the University. Revisions are to be recommended by the Board of Studies for **Electronics & Communication Engineering** and approved by the Academic Council.
Effective from	12-09-2022
Approvals	• Approved in the 50th meeting of Academic Council of NITTE (Deemed to be University), held on 30-05-2022 and vide Notification of NITTE (DU), N(DU)/REG/N-MCE/2022-23/76B dated 19-08-2022. • Notification of Nitte (DU), N(DU)/REG/AC/-SA/2022-23/909 dated 24-04-2023.
Program offered at	NMAM Institute of Technology, Nitte Off Campus centre, Nitte (Deemed to be University)
Grievance and dispute resolution	All disputes arising from this set of regulations shall be addressed to the Board of Management. The decision of the Board of Management is final and binding on all parties concerned. Further, any legal disputes arising out of this set of regulations shall be limited to jurisdiction of Courts of Mangalore only

Contents

1. INTRODUCTION:

1.1 The general regulations are common to all Degree of Master of Technology Program under Outcome Based Education (OBE) and Choice Based Credit System (CBCS) conducted by Nitte (Deemed to be University), at the NMAM Institute of Technology, Nitte off Campus Centre and shall be called "Nitte(DU) Regulations for M.Tech.- 2022".

1.2 The provisions contained in this set of regulations govern the policies and procedures on the Registration of students, imparting Instructions of course, conducting of the examination and evaluation and certification of students' performance and all amendments there to leading to the said degree program(s)

1.3 This set of Regulations, on approval by the Academic Council and Governing Council, shall supersede all the corresponding earlier sets of regulations of the M.Tech. Degree program (of Nitte (DU)) along with all the amendments thereto, and shall be binding on all students undergoing M.Tech. Degree Program (s) (Choice Based Credit System) conducted at the NMAMIT, Nitte with effect from its date of approval and is applicable for students admitted to 1st year after September 2022. This set of regulations may evolve and get modified or changed through appropriate approvals from the Academic Council / Governing Council from time to time, and shall be binding on all stake holders, (the Students, Faculty, Staff of Departments of NMAMIT, Nitte). The decision of the Academic Council/ Governing Council shall be final and binding.

1.4 In order to guarantee fairness and justice to the parties concerned in view of the periodic evolutionary refinements, any specific issues or matters of concern shall be addressed separately, by the appropriate authorities, as and when found necessary.

1.5 The Academic Council may consider any issues or matters of Concern relating to any or all the academic activities of the NMAMIT courses for appropriate action, irrespective of whether a reference is made here in this set of Regulations or otherwise.

1.6 The course shall be called **Master of Technology** program abbreviated as M.Tech. (subject of specialization) – Choice Based Credit System.

2. DEFINITIONS OF KEYWORDS:

The following are the definitions/descriptions that have been followed for the different terms used in the Regulations of M.Tech. Programs:

2.1 **Program:** Is an educational program in a particular stream/branch of Engineering/branch of specialization leading to award of Degree. It involves events/activities, comprising of lectures/ tutorials/ laboratory work/ field work, outreach activities/ project work/ vocational training/ viva/ seminars/ Internship/ assignments/ presentations/ self-study etc., or a combination of some of these.

2.2 **Branch:** Means Specialization or discipline of M. Tech Degree Program, like Electrical Vehicle Technology, Structural Engineering, Machine Design, etc.

2.3 **Semester:** Refers to one of the two sessions of an academic year (vide: serial number 4), each session being of sixteen weeks duration (with working days greater than or equal to 90). The odd semester may be scheduled from August/September and even semester from February/March of the year.

2.4 **Academic Year:** Refers to the sessions of two consecutive semesters (odd followed by an even) including periods of vacation.

2.5 **Course:** Refers to usually referred to as 'subjects' and is a component of a program. All Courses need not carry the same credit weightage. The Courses should define learning objectives and learning outcomes. A Course may be designed to comprise lectures/ tutorials/ laboratory work/ field work/ outreach activities/ project work/ vocational training/ viva/ seminars/ term papers/ assignments/ presentations/ self-study etc.. or a combination of some of these.

2.6 **Credit:** Refers to a unit by which the Course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of lecture or two hours of laboratory/ practical Courses/ tutorials/ fieldwork per week etc.

2.7 **Audit Courses:** Means Knowledge/ Skill enhancing Courses without the benefit of credit for a Course.

2.8 **Choice Based Credit System (CBCS):** Refers to customizing the Course work, through Core, Elective and soft skill Courses, to provide necessary support for the students to achieve their goals.

2.9 **Course Registration:** Refers to formal registration for the Courses of a semester (Credits) by every student under the supervision of a Faculty Advisor (also called Mentor, Counsellor etc.,) in each Semester for the Institution to maintain proper record.

2.10 **Course Evaluation:** Means Continuous Internal Evaluation (CIE) and Semester End Examinations (SEE) to constitute the major evaluations prescribed for each Course. CIE and SEE to carry 50 % and 50 % respectively, to enable each Course to be evaluated for 100 marks, irrespective of its Credits.

2.11 **Continuous Internal Evaluation (CIE):** Refers to evaluation of students' achievement in the learning process. CIE shall be by the Course Instructor and includes tests, homework, problem solving, group discussion, quiz, mini-project and seminar throughout the Semester, with weightage for the different components being fixed at the University level.

2.12 Semester End Examinations (SEE): Refers to examination conducted at the University level covering the entire Course Syllabus. For this purpose, Syllabi to be modularized and SEE questions to be set from each module, with a choice confined to the concerned module only. SEE is also termed as university examination.

2.13 Make Up Examination: Refers to examination conducted for the candidates who has a CIE>=35 marks and may have missed to attend the SEE covering the entire course syllabus. The standard of Make Up Examination is same as that of the SEE.

2.14 Supplementary Examination: Refers to the examination conducted to assist slow learners and/or failed students through make up courses for a duration of 8 weeks. This comprises of both the CIE & SEE and will be conducted after the completion of First year M.Tech. even semester.

2.15 Credit Based System (CBS): Refers to quantification of Course work, after a student completes teaching – learning process, followed by passing in both CIE and SEE. Under CBS, the requirement for awarding Degree is prescribed in terms of total number of credits to be earned by the students.

2.16 Credit Representation: Refers to Credit Values for different academic activities considered, as per the Table.1. Credits for seminar, project phases, project viva–voce and internship shall be as specified in the Scheme of Teaching and Examination.

Table 1: Credit Values

Theory/Lectures (L) (hours/week/Semester)	Tutorials (T) (hours/week/ Semester)	Laboratory /Practical (P) (hours/week/ Semester)	Credits (L: T:P)	Total Credits
4	0	0	4:0:0	4
3	0	0	3:0:0	3
2	2	0	2:1:0	3
2	0	2	2:0:1	3
2	2	2	2:1:1	4
0	0	2	0:0:1	1
NOTE: Activities like, practical training, study tour and participation in Guest lectures not to carry any credits.				

2.17 Letter Grade: It is an index of the performance of students in a said Course. Grades are denoted by letters O, A+, A, B+, B, C and F.

2.18 Grading: Grade refers to qualitative measure of achievement of a student in each Course, based on the percentage of marks secured in (CIE+SEE). Grading is done by Absolute Grading. The rubric attached to letter grades are as follows:

Letter Grade	O	A+	A	B+	B	C	F
Academic Level	Outstanding	Excellent	Very Good	Good	Above Average	Average	Fail

2.19 Grade Point (GP): Refers to a numerical weightage allotted to each letter grade on a 10-point scale as under.

Letter Grade and corresponding Grade Points on a typical 10 – Point scale							
Letter Grade	O	A+	A	B+	B	C	F
Grade Point	10	09	08	07	06	05	00

2.20 Passing Standards: Refers to passing a Course only when getting GP greater than or equal to 05 (as per serial number 2.20).

2.21 Credit Point: Is the product of grade point (GP) and number of credits for a Course i.e., Credit points CrP = GP × Credits for the Course.

2.22 Semester Grade Point Average (SGPA): Refers to a measure of academic performance of student/s in a semester. It is the ratio of total credit points secured by a student in various Courses of a semester and the total Course credits taken during that semester.

2.23 Cumulative Grade Point Average (CGPA): Is a measure of overall cumulative performance of a student over all semesters. The CGPA is the ratio of total credit points earned by a student in various Courses in all semesters and the sum of the total credits of all Courses in all the semesters. It is expressed up to two decimal places.

2.24 Grade Card: Refers to a certificate showing the grades earned by a student. A grade card shall be issued to all the registered students after every semester. The grade card will display the program details (Course code, title, number of credits, grades secured) along with SGPA of that semester and CGPA earned till that semester.

2.25 University: Nitte (Deemed to be University), Mangalore. NMAM Institute of Technology is an off-campus centre of Nitte (DU) and located at Nitte.

3. CLAUSE

CLAUSE	PARTICULARS
22NMT1.0	**DURATION AND CREDITS OF THE PROGRAM OF STUDY** There shall be one category of program: Full-time Program (FT) **Full-time Program:** The Program shall extend over a period of four semesters (2 years). First Semester: i) 16 weeks – Class Work according to the scheme. ii) 4 weeks – Revision holidays and examinations iii) 2 weeks – Vacation **Second Semester:** i) 16 weeks – Class Work according to the scheme ii) 4 weeks – Revision holidays and examinations. **Summer Semester/Vacation** i) 4 weeks — Class work, Examination & Display of Grades **Third Semester: 20 weeks** i) 8 weeks — Industrial Training/Mini Project ii) 12 weeks — Project Part-I — Industrial Training/Mini Project evaluation, Seminar on Special Topic Evaluation & Project Part-I Evaluation **Fourth Semester: 24 weeks** i) 22 weeks — Project Part-II ii) 2 weeks – Submission, viva -voce **Prescribed Number of Credits for the Program: 80** The number of credits to be completed for the award of Degree shall be 80.
22NMT1.1	M.Tech Degree Programs are offered in the following specialization and the respective program hosting departments are listed below:

Program	**Department**
i) Computer Science & Engineering	Computer Science & Engineering
ii) Constructional Technology	Civil Engineering
iii) Structural Engineering	Civil Engineering
iv) VLSI Design & Embedded Systems	Electronics and Communication Engineering

	<table><tr><td>v) Machine Design</td><td>Mechanical Engineering</td></tr><tr><td>vi) Energy Systems Engineering</td><td>Mechanical Engineering</td></tr><tr><td>vii) Cyber security</td><td>Computer Science Engineering</td></tr><tr><td>viii) Electric Vehicle Technology</td><td>Electrical and Electronics Engineering</td></tr></table> The provisions of these Regulations shall be applicable to any new specialization that may be introduced from time to time and appended to the above list.
22NMT1.2	**Maximum Duration for Program Completion:** A full-time candidate shall be allowed a maximum duration of 4 years from the I semester of admission to become eligible for the award of master's degree, failing which he/she may discontinue of register once again as a fresh candidate to I semester of the program.
22NMT2.0	**ELIGIBILITY FOR ADMISSION** (As per the Government orders issued from time to time): Admission to I year/ I semester Master of Technology Program shall be open to all the candidates who have passed B.E./ B. Tech. Examinations (in relevant field) or any other recognized University/ Institution. AMIE in respective branches shall be equivalent to B.E./ B. Tech. Programs for admission to M.Tech. The decision of the equivalence committee shall be the final in establishing the eligibility of candidates for a particular Program. For the foreign Degrees, Equivalence certificate from the Association of Indian Universities shall be a must.
22NMT2.1	Admission to M.Tech. Program shall be open to the candidates who have passed the prescribed qualifying examination with not less than 50% of the marks in the aggregate of all the years of the Degree examination. Rounding off percentage secured in qualifying examination is not permissible.
22NMT2.2	**For admissions under GATE/ NUCAT qualification** The candidates should be GATE qualified or should have appeared for the NUCAT Entrance Examination conducted by Nitte (Deemed to be University) [Nitte (DU)]
22NMT2.3	**For admissions under Sponsored Quota:**

	The candidates should be GATE qualified or should have appeared for the NUCAT Entrance Examination conducted by Nitte (DU)
22NMT2.4	The candidates, who are qualified in the GATE Examination for the appropriate branch of engineering, shall be given priority. They are exempted from taking NUCAT Entrance Examination. In case a GATE qualified Candidate appears for entrance examination and become qualified to claim a seat under entrance examination quota, he/she will be considered in the order of merit along with other candidates appeared for the entrance examination.
22NMT2.5	If sufficient number of GATE qualified candidates are not available, the remaining vacant seats shall be filled from amongst the candidates appeared for NUCAT Entrance Examination in the order of merit.
22NMT2.6	Engineering graduates other than the Karnataka candidates shall get their Eligibility verified from Nitte (DU) to seek admission to M.Tech. Program at NMAMIT, Nitte
22NMT2.7	**Admission to vacant seats:** Seats remaining vacant (unfilled), after the completion of admission process through GATE/NUCAT Entrance Exam, the remaining seats shall be filled by Candidates based on merit in the entrance test conducted at the Institution level. An admission Committee, consisting of the Principal, Head of the concerned Department and the subject experts, shall oversee admissions.
22NMT3.0	**REGISTRATION:** Every student after consulting his **Faculty-Advisor** in parent department is required to register for the **approved courses** with the **Departmental Post Graduate Committee (DPGC)** of Parent Department at the commencement of each Semester on the days fixed for such registration and notified in the academic calendar.
22NMT3.1	**Lower and Upper Limits for Course Credits Registered in a Semester. Course Credit Assignment:** All courses comprise of specific Lecture/ Tutorial/ Practical (L-T-P) schedule. The course credits are fixed based on the following norms. Lecture/Tutorials/ Practical: (i) a 1-hour Lecture per week is assigned 1.0 Credit.

(ii) a 2-hour Tutorial session per week is assigned 1.0 Credit.

(iii) a 2-hour Lab. session per week is assigned 1.0 credits

For example, a theory course with L-T-P schedule of 3-2-0 hours will be assigned 4.0 credits.

A laboratory practical course with L-T-P schedule of 0-0-2 hours will be assigned 1.0 credit.

Calculation of Contact Hours / Week – A Typical Example

Typical Academic Load (I & II Semester)				
No. of Courses	**LTP**	**Credits Per course**	**Total Credits**	**Contact Hours per**
2 Lecture Courses	4-0-0	04	08	08
2 Lab Courses	0-0-2	01	02	04
1 Research based Course	0-0-4	02	02	04
3 Elective Courses	3-0-0	03	09	09
1 Audit Course	2-0-0	0	0	02
Total: 9 Courses			21	27

A student must register, as advised by Faculty Advisor, between a minimum of 16 credits and up to a Maximum of 28 credits. However, the minimum/ maximum Credit limit can be relaxed by the Dean (Academic) on the recommendations of the DPGC, only under extremely exceptional circumstances.

22NMT3.2

Mandatory Pre-Registration for higher semester:

In order to facilitate proper planning of the academic activities of the Semester, it is necessary for the students to declare their intention to register for courses of higher semesters (2^{nd} and above) at least two weeks before the end of the current semester choosing the courses offered by each department in the next higher semester which is displayed on the Departmental Notice Board at least 4 weeks prior to the last working day of the semester. Students who fail to register on or before the specified date will have to pay a late fee. Registration in absentia is allowed only in exceptional cases with the permission of the Dean (Academic).

	Registration to a higher semester is allowed only if the student fulfills the following conditions- i) Satisfied all the academic requirements to continue with the program of studies without termination ii) Cleared all institute, hostel and library dues and fines, if any, of the previous semester. iii) Paid all required advance payments of the Institute and the hostel for the current semester. Has not been debarred from registering on any specific grounds by the Institute.
22NMT3.3	**Course Pre-Requisites:** In order for a student to register for some course(s), it may be required either to have completed satisfactorily or to have prior earned credits in some specified course(s). In such instances, the DPGC shall specify clearly, any such course pre-requisites, as part of the curriculum.
22NMT3.4	Students who do not register before the dead line day of registration may be permitted LATE Registration up to the notified day in academic calendar on payment of late fee.
22NMT3.5	REGISTRATION in ABSENTIA will be allowed only in exceptional cases on the recommendation of DPGC through the authorized representative of the student.
22NMT3.6	Medium of Instruction/Evaluation/etc. shall be English.
22NMT4.0	**COURSES:** The curriculum of the Program shall be any combination of following type of courses: i) **Professional Core Courses (PCC)** - relevant to the chosen specialization/ branch [May be split into Hard (no choice) and Soft (with choice), if required]. The core course is to be compulsorily studied by a student and is mandatory to complete the requirements of a program in a said discipline of study. ii) **Professional Electives Courses (PEC)** - relevant to the chosen specialization/ branch: these are the courses, which can be chosen from the pool of papers. It shall be supportive to the discipline/ providing

extended scope/enabling an exposure to some other discipline / domain / nurturing student skills.

iii) **Research Experience** Through Practice-I and Research Experience Through Practice-II

iv) **Project Work**

v) **Seminar**

vi) **Audit Courses (AC):**

a) The Audit course can be any credit course offered by the program to which the candidate is admitted (other than the courses considered for completing the prescribed program credits) or other programs offered in the institution, where the student is studying.

b) The students are required to register for one audit course during I and II semesters. Students who have registered to audit the courses, considered on par with students registered to the same course for credit, must satisfy attendance and CIE requirements. However, they need not have to appear for SEE.

c) Registration for any audit course shall be completed at the beginning of I and II semesters. The Department should intimate the Controller of Examination about the registration at the beginning of the semester and obtain a formal approval for inclusion of the audit course/s in the Grade card issued to the students

vii) **Internship/ Mini Project:** Preferably at an industry/ R&D organization/IT company/ Government organization of significant repute or at the Research Centre of parent Institution for a specified period mentioned in Scheme of Teaching and Examination.

22NMT4.1

Program Structure:

The number of credits to be registered in a semester is between 16 and 28

Minimum Credit Requirement for the M.Tech. Degree is 80.

The total course package for an M.Tech. Degree Program will typically consist of the following components.

Course type	Range %	Suggested Credits

i) Program Core Courses	20 - 25	20
ii) Program Elective Courses	18 - 20	15
iii) Elective Courses (MOOCS)	4	03
iv) Industrial Internship/Research Internship/Mini Project	10	08
v) Project	35	28
vi) Seminar	2.5	02
vii) Research Experience Through Practice	5	04
viii) Audit courses (two courses)	-	-
Total credits		80

The Department Post Graduate Committee (DPGC) will discuss and recommend the exact credits offered for the program for the above components, the semester-wise distribution among them, as well as the syllabi of all postgraduate courses offered by the department from time to time before sending the same to the Board of Studies (BOS).

The BOS will consider the proposals from the departments and make recommendations to the Academic Council for consideration and approval.

Mandatory Learning Courses:

These are courses that must be completed by the student at appropriate time as suggested by the Faculty Adviser or the DPGC. Courses that come under the category are as following:

Industrial Training:

This is a 08-credit course. A full-time student will complete the Industrial Training (or a Mini Project) at appropriate time stipulated by DPGC and register for it in the following Semester and shall also submit a bound copy of training report certified by the authority of Training Organization. The duration and the details, including the assessment scheme, shall be decided by the faculty advisor, with approval from DPGC.

Seminar:

	This also carries 2-credits to be completed at appropriate time stipulated by DPGC. The student will make presentations on topics of academic interest, as suggested by DPGC. **Research Experience through Practice-I and Research Experience through Practice-II:** • Research Experience through Practice-I and II are 2-credit courses in the first and second semesters respectively. • The student will work under a faculty supervisor approved by the DPGC and submits a research proposal at the end of the first semester which is evaluated jointly by the faculty supervisor and a co-examiner. • Students shall be offered inputs like how to conduct a literature survey, how to identify a research problem, how to write a research paper, research report, research proposal, and systematic way of conducting research etc. • Department specific/PG Program specific skill sets required for carrying out a research work may be offered to the students like software tools for system/device simulation and analysis, software/ hardware tools for signal acquisition, data processing, control simulation, Testing/measuring equipment used in research and Testing/measuring procedure. • At the end of Research Experience through Practice-I in the first semester, M. Tech. students should be able to identify a research problem, with clear objectives and methodologies backed by extensive literature review. • Two internal examiners will evaluate the Research Experience through Practice-I out of which one will be the guide and the other examiner will a faculty member who is having expertise in the research area of the student being evaluated. The research proposal report and the research proposal presentation are evaluated for 100 marks in the first semester. • The student will work on the proposed research in the second semester and submit a research paper at the end of the second semester which is evaluated jointly by the faculty supervisor and a co-examiner. • In the second semester, the students are expected to carry out Mathematical modelling / Design calculations / computer simulations / Preliminary experimentation / testing of the research problems identified during Research Experience through Practice-I carried out in the first

	semester. At the end of the second semester, students are expected to write a full research paper based on the Mathematical modelling/ Design calculations/computer simulations/Preliminary experimentation/testing carried out during second semester. The research paper submitted by the student and the presentation of the research work carried out is evaluated for 100 marks in the second semester.
22NMT5.0	**INTERNSHIP/MINI PROJECT:** The student shall undergo Internship/Mini Project as per the Scheme of Teaching and Examination. 1. The internship can be carried out in any industry/R&D Organization/Research Institute/Institute of national repute/R&D Centre of Parent Institute. 2. The Department/college shall nominate a faculty to facilitate, guide and supervise students under internship. 3. The students shall report the progress of the internship/Mini Project to the internal guide in regular intervals and seek his/her advice. 4. The Internship shall be completed during the period specified in Scheme of Teaching and Examination. 5. After completion of Internship/mini project, students shall submit a report to the Head of the Department with the approval of both internal and external guides and with the approval of internal guide if the Internship/Mini-Project is carried out in the Institute. 6. The Internship/Mini Project will be evaluated jointly by two internal examiners appointed by the Head of the Department/Controller of Examination. 7. The Internship/Mini Project report and the presentation by the student will be evaluated for 50 marks each immediately after completion of the Internship/Mini Project. The students are permitted to carry out the internship anywhere in India or Abroad. The Institution will not provide any kind of Financial Assistance to any student for Internship/Mini Project and for the conduct of Viva-Voce on internship.
22NMT5.1	**Failing to undergo Internship/Mini Project:**

	Securing a pass grade in Internship/Mini Project is mandatory as a partial requirement for the award of Degree. Internship/Mini Project Securing a pass grade in Internship/Mini Project is mandatory. If any student fails to undergo/complete the Internship/Mini Project, he/she shall be considered as fail in that Course.
22NMT6.0	**SEMINAR:** Securing a pass grade in Seminar is mandatory as a partial requirement for the award of Degree. i) Each candidate shall deliver seminar as per the Scheme of Teaching and Examination on the topics chosen from the relevant fields for about 30 minutes. The Head of the Department shall make arrangements for conducting seminars through concerned faculty members of the department. The Panel of Examiners constituted for the purpose by the Head of the Department shall award the CIE marks for the seminar.
22NMT7.0	**PROJECT WORK:** Securing a pass grade in Project Work is mandatory as a partial requirement for the award of Degree. Project work shall be on individual basis. **Project Part-I and Part-II:** **Project Part-I: (In third Semester)** The duration of the Project Part-I is of 12 weeks as notified in the academic calendar. The evaluation of the Project Part-I will be done during the end of third semester. Each department will prepare the Panel of Examiners in advance and also prepare the Project Part-I evaluation schedule indicating the names of the students, their USN, Title of the Project, Name of the Examiners, and time and Venue of the evaluation which will be submitted to the Controller of Examination Office in advance. Project Part-I evaluation will be done by two internal Examiners, one of them will be the Guide and other is preferably one of the experts in the area of PG Project being evaluated.

	The mark distribution of Project Phase-I evaluation is: 100 marks for report and 100 marks for presentation jointly awarded by the both the examiners. **Project Part-II: (In the fourth Semester)** The total duration of Project Part-II is of 22 weeks as notified in the academic calendar. There will be two Continuous Internal Evaluation of Project Part-II in fourth semester followed by Semester End Evaluation of the Project Phase-II, namely, Project Progress Evaluation-I (PPE-I), Project Progress Evaluation -II(PPE-II) and SEE. The same Panel of Examiners which was formed during Project Part-I evaluation is to be continued for the Project Progress Evaluation in the fourth semester. PPE-I and PPE-II will be scheduled as per the academic calendar and will be evaluated for 100 marks each (50 marks for report and 50 marks for presentation jointly conducted by the two internal examiners). Each department will prepare the Panel of Examiners in advance and also prepare the Project Part-II Project Progress Evaluation Schedule indicating the names of the students, their USN, Title of the Project, Name of the Examiners, and time and Venue of the evaluation as per the format which will be submitted to the Controller of Examination Office in advance. For the Off-Campus projects, the Internal Guide should visit the organization in which the M.Tech Student is carrying out his Project at least once during the project term. The candidate shall submit a soft copy of the dissertation work to the Institute. The soft copy of the dissertation should contain the entire Dissertation in monolithic form as a PDF file (not separate chapters). The Guide, after checking the report for completeness shall check the report for Plagiarism content. The allowable plagiarism index is less than or equal to 25%. If the check indicates a plagiarism index greater than 25%, the guide should advice the student to resubmit the dissertation after modifying the report. The report has to be once again checked for the plagiarism content and the signed hard copy of the Plagiarism Report along with the two hard copies of the dissertation is to be submitted to the Head of the Institution through the Head of the Department. The dissertation will be evaluated by two examiners,

	one of the examiners shall be the Guide of the candidate and the other examiner shall be an external expert in the area of the dissertation being evaluated. The guide shall submit panel of two approved external examiners to the office of the Controller of Examination through the head of the Department. The Controller of Examination will randomly select one of the external examiners and invites him/her formally for the evaluation of the dissertation and Viva-Voce examination giving sufficient time for the external examiner for reading the dissertation.
22NMT7.1	The dissertation will be evaluated by two examiners, one of the examiners shall be the guide of the candidate and the other examiner shall be preferably an external expert in the area of the dissertation being evaluated. The evaluation of the dissertation shall be made independently by each examiner.
22NMT7.2	Examiners shall evaluate the dissertation normally within a period of not more than two weeks from the date of receipt of dissertation through email.
22NMT7.3	The examiners shall independently submit the marks for the dissertation during the viva-voce examination date
22NMT7.4	Sum of the marks awarded by the two examiners shall be the final evaluation marks for the Dissertation.
22NMT7.5	(a) Viva-voce examination of the candidate shall be conducted, if the dissertation work and the reports are accepted by the external examiner. (b) If the external examiner finds that the dissertation work is not up to the expected standard and the minimum passing marks cannot be awarded, the dissertation shall not be accepted for SEE. (c) If the dissertation is rejected during the Project Part II, then the Second Examiner (external) will be appointed by the COE against whom the candidate has to re-present the same dissertation. The decision of the Second Examiner (external) will be final. If the second examiner (external) accepts the dissertation, then the viva-voce examination of the candidate shall be conducted as per the norms. If the second examiner (external) rejects the dissertation, then the student has to take an extension for a minimum period of 3 months and re-work on the project. After the completion of the extension period, viva-voce examination of the

	candidate shall be conducted as per the norms, if the dissertation work is accepted by the external examiner.
22NMT7.6	The candidate, whose dissertation is rejected, can rework on the same topic or choose another topic of dissertation under the same Guide or new Guide if necessary. In such an event, the report shall be submitted within four years from the date of admission to the Program.
22NMT7.7	Viva-voce examination of the candidate shall be conducted jointly by the external examiner and internal examiner/ guide at a mutually convenient date.
22NMT7.8	The relative weightages for the evaluation of dissertation and the performance at the viva-voce shall be as per the scheme of teaching and examination.
22NMT7.9	The marks awarded by both the Examiners at the viva-voce Examination shall be sent jointly to the office of Controller of Examination immediately after the examination.
22NMT7.10	Examination fee as fixed from time to time by the Institute for evaluation of dissertation report and conduct of viva-voce shall be remitted to the Institute as per the instructions of Dean-Academics, from time to time.
22NMT7.11	The candidates who fail to submit the dissertation work within the stipulated time have to apply for the extension of the Project duration through the Guide and the head of the department to the Office of the Controller of Examination. Such candidate is not eligible to be considered for the award of rank.
22NMT8.0	**ATTENDANCE REQUIREMENT:** 1. Each semester is considered as a unit and the candidate has to put in a minimum attendance of 85% in each subject with a provision of condoning 10% of the attendance by Principal for reasons such as medical grounds, participation in University level sports, cultural activities, seminars, workshops and paper presentation etc. 2. The basis for the calculation of the attendance shall be the period of term prescribed by the institution in its calendar of events. For the first semester students, the same is reckoned from the date of admission to the course 3. The students shall be informed about their attendance position in the first week of every month by the College so that the students shall be cautioned to make up the shortage.

	4. The head of the department shall notify regularly, the list of such candidates who fall short of attendance. The list of the candidates falling short of attendance shall be sent to the Principal with a copy to Controller of Examinations. 5. A candidate having shortage of attendance (<75%) in any course(s) registered shall not be allowed to appear for SEE of such course(s). Such students will be awarded 'N' grade in these courses. 6. He/she shall have to repeat those course(s) with 'N' grade and shall re-register for the same course(s) core or elective, as the case may be when the particular course is offered next either in a main (odd/even) or summer semester. 7. If a candidate, for any reason, discontinues the course in the middle he/she may be permitted to register to continue the course along with subsequent batch, subject to the condition that he/she shall complete the class work, lab work and seminar including the submission of dissertation within maximum stipulated period. Such candidate is not eligible to be considered for the award of rank.
22NMT9.0	**ADD/ DROP/ AUDIT OPTIONS:** 1. ADD-option: A student has the option to ADD courses for registration till the date specified for late registration. 2. DROP-option: A student has the option to DROP courses from registration until one week after the mid-semester examination. AUDIT-option: A student can register for auditing a course, or a course can even be converted from credit to audit or from audit to credit, with the consent of faculty advisor and course instructor until one week after the mid-semester exam. However, CORE courses shall not be made available for audit. It is not mandatory for the student to go through the regular process of evaluation in an audit course. However, the student has to keep the minimum attendance requirement, as stipulated by the corresponding DPGC for getting the 'U' grade awarded in a course, failing which that course will not be listed in the Grade Card.
22NMT10.0	**ABSENCE DURING THE SEMESTER:** **Leave of Absence**

	(a) If the period of leave is more than two days and less than three weeks, prior application for leave shall have to be submitted to the Head of the Department concerned, with the recommendation of the Faculty-Advisor stating fully the reasons for the leave request along with supporting documents. It will be the responsibility of the student to intimate the course instructors, Head of the Department and also Chief Warden of the hostel, regarding his absence before availing leave.
22NMT10.1	**Absence during Mid-Semester Examinations:** A student who has been absent from a Mid-Semester Examination (MSE) due to illness and other contingencies may give a request for additional MSE within two working days of such absence to the office of the respective Head of the Department (HOD) with necessary supporting documents and certification from authorized personnel. The HOD may consider such requests depending on the merits of the case, may permit the additional Mid-Semester Examination for the concerned student.
22NMT10.2	**Absence during Semester End Examination:** In case of absence for a Semester End Examination, on medical grounds or other special circumstances the student can apply for 'I' grade in that course with necessary supporting documents and certifications by authorized personnel to the Controller of Examination through Chairman of The Department. The Controller of Examination may consider the request depending on the merits of the case and permit the make-up Semester End Examination for the concerned student. The student may subsequently complete all course requirements within the date stipulated by DPGC (which may be extended till first week of next semester under special circumstances) and 'I' grade will then be converted to an appropriate letter grade. If such an application for the 'I' grade is not made by the student, then a letter grade will be awarded based on his in-semester performance.
22NMT11.0	**WITHDRAWAL FROM THE PROGRAM:** **Temporary Withdrawal:** A student who has been admitted to a Post Graduate Degree program of the College may be permitted to withdraw

	temporarily, for a period of one semester or more on the grounds of prolonged illness or grave calamity in the family etc. The student should abide by the applicable rules and regulations of the college/University at the time of Temporary Withdrawal.
22NMT11.1	**Permanent Withdrawal:** Any student who withdraws admission before the closing date of admission for the Academic Session is eligible for the refund of the deposits only. Fees once paid will not be refunded on any account. Once the admission for the year is closed, the following conditions govern withdrawal of admissions: a) A student who wants to leave the College for good, will be permitted to do so (and can take Transfer Certificate from the College, if needed), only after remitting the Tuition fees as applicable for all the remaining semesters and clearing all other dues, if any. b) Those students who have received any scholarship, stipend or other forms of assistance from the College shall repay all such amounts in addition to those mentioned in (a) above. The decision of the Principal of the Institute regarding withdrawal of a student is final and binding.
22NMT12.0	**EVALUATION SYSTEM:** **Continuous Internal Evaluation (CIE) and Semester End Evaluation (SEE)**
22NMT12.1	For all the theory and laboratory courses, the CIE marks shall be 50. For Research Experience through Practice-I, Research Experience through Practice-II, Seminar, Industrial Training/Mini Project, the CIE marks shall be 100. For Project Phase-I, the CIE Marks shall be 200 For Project Phase-II, the CIE Marks shall be 200 and for SEE 200
22NMT12.2	CIE Marks for courses shall be based on a) Tests MSE-I and MSE-II (for 30 Marks): MSE in a theory course, for 30 marks, shall be based on two tests covering the entire syllabus. Assignments, Quizzes, Simulations, Experimentations, Mini project, oral examinations, field work etc., (for 20 Marks) conducted in respective courses.

22NMT12.3	a) An additional MSE may be conducted for those students absent for valid reasons/ with prior permission. b) For those students who could not score minimum required CIE marks (25 marks), an additional MSE may be conducted, however the maximum CIE marks shall be restricted to 25 out of 50.
22NMT12.4	The candidates shall write the Tests in Blue Book/s. The Blue book/s and other documents relating to award of CIE marks shall be preserved by the Head of the Department for at least six months after the announcement of University results and made available for verification at the directions of the Controller of Examination.
22NMT12.5	Every page of the CIE marks list shall bear the signatures of the concerned Teacher and Head of the Department.
22NMT12.6	The CIE marks list shall be displayed on the Notice Board and corrections, if any, shall be incorporated before submitting to the office of the Controller of Examination (COE).
22NMT12.7	The CIE marks shall be sent to the office of the COE well in advance before the commencement of Semester End Examinations. No corrections of the CIE marks shall be entertained after the submission of marks list to the Office of the COE.
22NMT12.8	Candidates obtaining less than 50% of the CIE marks in any course (Theory /Laboratory/ Seminar/ Internship/ Project) shall not be eligible to appear for the Semester end examination in that course/s. In such cases, the Head of the Department shall arrange for the improvement of CIE marks in the course/ Laboratory when offered in the subsequent semester subject to the maximum duration allowed for completion of a M.Tech. program.
22NMT12.9	**Semester End Evaluation:** There shall be a Semester End Examination at the end of each semester.
22NMT12.10	There shall be double valuation of theory papers. The theory Answer booklets shall be valued independently by two examiners appointed by the Controller of Examination.
22NMT12.11	If the difference between the marks awarded by the two examiners is not more than 15 per cent of the maximum marks, the marks awarded to the candidate shall be the average of two evaluations.

22NMT12.12	If the difference between the marks awarded by the two examiners is more than 15 per cent of the maximum marks, the answer booklet shall be evaluated by a third Examiner appointed by the Controller of Examination. The average of the marks of nearest two valuations shall be considered as the marks secured by the candidate. In case, if one of the three marks falls exactly midway between the other two, then the highest two marks shall be taken for averaging.
22NMT12.13	**Summer Semester:** Summer semester is primarily to assist weak and/or students having N/F grade in courses, for a duration of 4 weeks after the completion of regular even SEE. The institute may also offer Add-on/ Audit Courses during this semester.
22NMT12.14	Each candidate shall obtain not less than 50% of the maximum marks (25 marks) prescribed for the CIE of each subject, including seminars. CIE Marks shall be based on assignments, tests, oral examinations and seminar (minimum of two are compulsory) conducted in respective subjects. The candidates obtaining less than 50% of the CIE marks in any subject shall not be eligible to appear for the SEE in that subject(s). Only in such cases, the Controller of Examination may arrange for reregistering the subject(s) in subsequent semester or may refer to DPGC for necessary remedial measures. The candidates shall write the Internal Assessment Test in Blue Books, and this shall be maintained by the Head of the Department for at least six months after the announcement of result and is available for verification. The CIE marks sheet shall bear the signature of the concerned Teacher and the Chairman of the Department. The CIE marks list shall be displayed on the Notice Board and corrections, if any, shall be incorporated before sending to the Controller of Examinations.
22NMT12.15	The Academic Performance Evaluation of a student shall be according to a Letter Grading System, based on the Class Performance Distribution. The Letter grades O, A+, A, B+, B, C and F indicate the level of academic achievement, assessed on a decimal (0-10) scale. The Letter grade awarded to a student in a course, for which he has registered shall be based on his performance in quizzes, tutorials, assignments etc., as applicable, in addition

	to two mid-semester examination and one semester end examination. The distribution of weightage among these components may be as follows: Semester End Examination (SEE) 50% Continuous Internal Evaluation (CIE) (i) Quizzes, Tutorials, Assignments etc., 20% (ii) Mid-semester Examination: 30% Any variation, other than the above distribution, requires the approval of the pertinent DPGC and Academic Council. The letter grade awarded to a student in a 0-0-P (Practical) course, is based on an appropriate continuous evaluation scheme that the course instructor shall evolve, with the approval of the pertinent DPGC. The course Instructor shall announce in the class, and/or display in the display boards or at the website, the details of the Evaluation Scheme, including the distribution of the weightage for each of the components, and method of conversion from the raw scores to the letter-grades; within the first week of the semester in which the course is offered, so that there are no ambiguities in communicating the same to all the students concerned.
22NMT12.16	**The Transitional Grades** 'I', 'W' and 'X' would be awarded in the following cases. These would be converted into one or the other of the letter grades (O-F) after the student completes the course requirements. **Grade "I":** To a student having attendance ≥85% and CIE ≥ 70%, in a course, but remained absent from SEE for valid & convincing reasons acceptable to the College, like: i. Illness or accident, which disabled him/her from attending SEE. ii. A calamity in the family at the time of SEE, which required the student to be away from the College. iii. However, the committee chaired by the Principal is authorized to relax the requirement of CIE ≥ 70% if the student is hospitalized or advised long term rest after discharge from the hospital by the Doctor. iv. Students who remain absent for Semester End Examinations due to valid reasons and those who are absent due to health reasons are required to submit the necessary documents along with their request to the Controller of Examinations to write Make up Examinations within

	2 working days of that examination for which he or she is absent, failing which they will not be given permission. • **Grade "W":** To a student having satisfactory attendance at classes but withdrawing from that course before the prescribed date in a semester as per Faculty Advice. • **Grade "X":** To a student having attendance ≥85% and CIE ≥ 70%, in a course but SEE performance could result in a 'F' grade in the course. (No "F" grade awarded in this case, but student's performance record will be maintained separately).
22NMT12.17	**The Make Up Examination** facility would be available to students who may have missed to attend the SEE of one or more courses in a semester for valid reasons and given the 'I' grade. Also, students having the 'X' grade shall also be eligible to take advantage of this facility. The makeup examination would be held as per dates notified in the Academic Calendar. However, it should be made possible to hold a make-up examination at any other time in the semester with the permission of the Academic Council of the College. In all these cases, the standard of SEE would be the same as the normal SEE.
22NMT12.18	All the 'W' grades awarded to the students would be eligible for conversion to the appropriate letter grades only after the concerned students re-register for these courses in a main/summer semester and fulfil the passing standards for their CIE and (CIE+SEE).
22NMT12.19	The suggested passing standards are CIE to have >=50% and CIE+SEE to have a grade better or at least equal to C. For maintaining high standards, the students scoring less than 50% in CIE are advised to withdraw and to reregister for the course when offered next. The letter grade 'W' to be entered in the grade card against the subject and not to be taken into account while calculating SGPA & CGPA
22NMT12.20	**Rules for grace marks** Grace marks up to 1% of the maximum total marks of the courses for which he/she is eligible and have registered (non-credit courses excluded) in the examination or 10 marks whichever is less shall be awarded to the failed course(s), (with a restriction of a maximum of 5 marks per course) provided on the award of such grace marks the candidate passes in that course(s)

22NMT13.0

LETTER GRADES AND GRADE POINTS:

The Institute adopts absolute grading system wherein the marks are converted to grades, and every semester result will be declared with semester grade point average (SGPA) and Cumulative Grade Point Average (CGPA). The CGPA will be calculated for every semester, except for the first semester.

The grading system with the letter grades and the assigned range of marks under absolute grading system are as given below:

Letter Grade	Grade-Points	Raw Scores %	Level of Academic Achievement
O	10	≥90	Out standing
A+	09	80-89	Excellent
A	08	70-79	Very Good
B+	07	60-69	Good
B	06	55-59	Above average
C	05	50-54	Average
F	00	<50	Fail
U			Audited

A student obtaining Grade F in a Course shall be considered fail and is required to reappear in subsequent SEE. Whatever the letter grade secured by the student during his /her reappearance shall be retained. However, the number of attempts taken to clear a Course shall be indicated in the grade cards/ transcripts.

Earned Credits:

This refers to the credits assigned to the course in which a student has obtained any one of the letter grades O, A+ A, B+, B and C

22NMT14.0

PROMOTION AND ELIGIBILITY:

22NMT14.1

Promotion:

a) All students are promoted to their next semester or year of their program, irrespective of the academic performance.

However, for submission for M.Tech. Major Project report in 4th semester, student should have completed all the courses up to 3rd semester

22NMT14.2	**The mandatory non-credit courses,** if any, shall not be considered for the award of class, calculation of SGPA and CGPA. However, a pass grade (PP) in the above courses is mandatory for the award of Degree.
22NMT15.0	**ELIGIBILITY FOR PASSING AND AWARD OF DEGREE:**
22NMT15.1	1. A student who obtains any grade O to C shall be considered as passed and if a student secures F grade in any of the head of passing, he/she has to reappear in that head for SEE 2. A student shall be declared successful at the end of the program for the award of Degree only on obtaining CGPA≥5.00, with none of the courses remaining with F grade. In case, the CGPA falls below 5.00, the student shall be permitted to appear again for SEE for required number of courses (other than seminar and practical) and times, subject to the provision of University, to make up CGPA≥5.0. The student should reject the SEE results of previous attempt and obtain written permission form the Controller of Examinations to reappear to the subsequent SEE.
22NMT15.2	For a pass in a theory course, the student shall secure a minimum of 40% of the maximum marks prescribed in the Semester End Examination and 50% of marks in CIE and 50% in the aggregate of CIE and SEE marks. The minimum passing grade in a course is C.
22NMT15.3	For a pass in Internship/ Practical/ Project/ Dissertation/ Viva-voce examination, a student shall secure a minimum of 50% of the maximum marks prescribed for the SEE in Internship/ Practical/ Project/ Dissertation/ Viva-voce. The minimum passing grade in a course is C.
22NMT15.4	For a pass, a candidate shall obtain a minimum of 50% of maximum marks in Seminar.
22NMT15.5	IV Semester full time candidates having backlog courses are permitted to upload the dissertation report and to appear for SEE. The IV semester grade card shall be released only when the candidate completes all the backlog courses and become eligible for the award of Degree.
22NMT15.6	**Eligibility for Award of Degree:** A student shall be declared to have completed the Degree of Master of Technology, provided the student has undergone the stipulated course work

	as per the regulations and has earned the prescribed credits, as per the scheme of teaching and examination of the program
22NMT16.0	**EVALUATION OF PERFORMANCE:** **Computation of SGPA and CGPA** SGPA and CGPA: The credit index can be used further for calculating the Semester Grade Point Average (SGPA) and the Cumulative Grade Point Average (CGPA), both being important academic performance indices of the student. While SGPA is equal to the credit index for a semester divided by the total number of credits registered by the student in that semester, CGPA gives the sum total of credit indices of all the previous semesters divided by the total number of credits registered in all these semesters. Both the equations together facilitate the declaration of academic performance of a student, at the end of a semester and at the end of successive semesters respectively SGPA is computed as follows: $$SGPA = \frac{\sum[(Course\ Credits) \times (Grade\ Point)]\ \text{(for all courses with letter grades including F grades in that semester)}}{\sum[Course\ Credits]\ \text{(for all courses with letter grades including F grades in that semester)}}$$ CGPA is computed as follows: $$CGPA = \frac{\sum[(Course\ Credits) \times (Grade\ Point)]\ \text{(for all courses excluding those with F grades until that semester)}}{\sum[Course\ Credits]\ \text{(for all courses excluding those with F grades until that semester)}}$$
22NMT16.1	**Communication of Grades:** • The SGPA and CGPA respectively, facilitate the declaration of academic performance of a student at the end of a semester and at the end of successive semesters. Both of them would be normally calculated to the second decimal position, so that the CGPA, in particular, can be made use of in rank ordering the students' performance in the Institute. If two students get the same CGPA, the tie could be resolved by considering the number of times a student has obtained higher SGPA, But, if it is still not

	resolved, the number of times a student has obtained higher grades like O, A, B etc. could be taken into account.
22NMT16.2	**Challenge evaluation** If a student is not satisfied with the marks allotted to him/her in the semester end examinations, he/she could apply for challenge evaluation within the prescribed time specified. In such cases the answer papers will be valued by the DPGC committee and marks secured by the students in the challenge evaluation will be final.
22NMT16.3	**Grade Card:** Based on the secured letter grades, grade points, SGPA and CGPA, a grade card for each semester shall be issued. On specific request on paying prescribed fee, a transcript indicating the performance in all semesters may be issued.
22NMT16.4	**Conversions of Grades into Percentage and Class Equivalence** Conversion formula for the conversion of CGPA into percentage is given below: Percentage of marks secured, P = CGPA Earned × 10 **Illustration: for CGPA of 8.18**: P = CGPA Earned 8.18 × 10 = 81.8 %
22NMT17.0	**DEGREE REQUIREMENTS:** The Degree requirements of a student for the M.Tech Degree program are as follows: 1. College Requirements: i) Minimum Earned Credit Requirement for M.Tech. Degree is 80 ii) Satisfactory completion of all Mandatory Learning courses 2. Program Requirements: i) Minimum Earned Credit Requirements on all core courses, ii) Elective Courses and major project as specified by the DPGC. The maximum duration for a student for complying to the Degree requirements is 8 semesters from the date of first registration for his first semester.
22NMT18.0	**TERMINATION FROM THE PROGRAM/READMISSION:** A student shall be required to leave the College without the award of the Degree, under the following circumstances: ii) Failing to complete the degree requirements in double the duration of the program

<table>
<tr><td></td><td>Based on disciplinary action suggested by the Academic Council/Governing Council.</td></tr>
<tr><td>22NMT19.0</td><td>GRADUATION REQUIREMENTS AND CONVOCATION:
1. A student shall be declared to be eligible for the award of the Degree if he has
a) Fulfilled Degree Requirements
b) No Dues to the College, Departments, Hostels, Library Central Computer Centre and any other center
c) No disciplinary action pending against him.
2. The award of the Degree must be recommended by the Academic council and approved by Governing Council of Nitte (DU)
Convocation: Degree will be awarded in person for the students who have graduated during the preceding academic year. Degrees will be awarded in absentia to such students who are unable to attend the Convocation. Students are required to apply for the Convocation along with the prescribed fees, after having satisfactorily completed all the Degree requirements within the specified date in order to arrange for the award of the Degree during convocation.</td></tr>
<tr><td>22NMT20.0</td><td>AWARD OF CLASS, PRIZES, MEDALS & RANKS:
• Award of Class: Sometimes, it would be necessary to provide equivalence of SGPA and CGPA with the percentages and/or Class awarded as in the conventional system of declaring the results of University examinations. This can be done by prescribing certain specific thresholds in these averages for Distinction, First Class and Second Class as described below.
Percentage Equivalence of Grade Points (For a 10-Point Scale)
<table>
<tr><th>GPA</th><th>Percentage of Marks*</th><th>Class</th></tr>
<tr><td>≥ 7.00</td><td>≥ 70%</td><td>Distinction</td></tr>
<tr><td>≥ 6.00</td><td>≥ 60%</td><td>First Class</td></tr>
<tr><td>5.0 ≥ GPA <6.00</td><td>50≥ Percentage < 60%</td><td>Second Class</td></tr>
</table>
Percentage * = (GPA) x 10</td></tr>
</table>

	• **For the award of Prizes, Medals and ranks**: The conditions stipulated by the Donor may be considered as per the statutes framed by the University for such awards. o An attempt means the appearance/registration of a candidate for an examination in one or more courses either in part or failing a particular examination. o A candidate who fails/remaining absent (after submitting exam application) in the main examination and passes one or more subjects/courses or all subjects/courses in the supplementary/Make-up examination such candidates shall be considered as taken more than an attempt. o Merit Certificates and University Medals/ will be awarded on the basis of overall CGPA, governed by the specific selection criteria that may be formulated by the University for such Medals / Awards o Only those candidates who have completed the Program and fulfilled all the requirements in the minimum number of years prescribed (i.e., 2 years) and who have passed each semester in the first attempt are eligible for the award of Merit Certificates and /or Ranks and University Medals. Candidates with W, N, I, X & F grades and who passes the courses in the subsequent/supplementary/make up examinations are not eligible for the award of Gold Medal or Merit Certificate.
22NMT21.0	**CONDUCT AND DISCIPLINE:** 1. Students shall conduct themselves within and outside the premises of the Institute, in a manner befitting the students of an Institution of National Importance 2. **As per the order of Honorable Supreme Court of India, ragging in any form is considered as a criminal offence and is banned, any form of ragging will be severely dealt with**. 3. The following acts of omission/ or commission shall constitute gross Violation of the code of conduct and are liable to invoke disciplinary measures: a) Ragging

b) Lack of courtesy and decorum; indecent behavior anywhere within or outside the campus.
c) Willful damage or stealthy removal of any property /belongings of the Institute /Hostel or of fellow students/ citizens
d) Possession, consumption or distribution of alcoholic drinks or any kind of hallucinogenic drugs.
e) Mutilation or unauthorized possession of Library books.
f) Noisy and unseemly behavior, disturbing studies of fellow Students.
g) Hacking in computer systems (such as entering into other Person's area without prior permission, manipulation and/or Damage of computer hardware and software or any other Cybercrime etc.,).
h) Plagiarism of any nature.
i) Any other act of gross indiscipline as decided by the University from time to time.
j) Smoking in College Campus and supari chewing.
k) Unauthorized fund raising and promoting sales

4. Commensurate with the gravity of offense, the punishment may be: reprimand, expulsion from the hostel, debarment from an examination, disallowing the use of certain facilities of the College, rustication for a specified period or even outright expulsion from the College, or even handing over the case to appropriate law enforcement authorities or the judiciary, as required by the circumstances.
   i) For an offence committed in
      a) A hostel
      b) A department or in a classroom
      c) Elsewhere,

      the Chief Warden, the Head of the Department and the Dean (Students Welfare), respectively, shall have the authority to reprimand or impose fine.
   ii) All cases involving punishment shall be reported to the Principal.
5. Cases of adoption of unfair means and/or any malpractice in an examination shall be reported to the Controller of Examination.

	○ **Note:** Students are required to be inside the examination hall 20 minutes before the commencement of examination. This is applicable for all examinations (Semester end/Supplementary/makeup) henceforth. Students will not be allowed inside the examination hall after the commencement, under any circumstances.

NITTE (Deemed to be University) | NMAM INSTITUTE OF TECHNOLOGY

Scheme & Syllabus for

M. Tech. (VLSI Design and Embedded Systems)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

2022-24

M. Tech. in VLSI Design and Embedded Systems

CREDIT DISTRIBUTION

No.	Course Category	Suggested Credits
1.	Professional Courses (PCC) – core	16
2.	Professional Courses (PEC) – elective	18
3.	Research Methodology & IPR/RETP	04
4.	Labs	04
5.	Project Work (UCC) (Phase 1 & 2)	08+20
6.	Audit Courses (2 Nos)	00
7.	Seminar on Current Topic (UCC)	02
8.	Internship (UCC)	08
	Total Credits to be earned:	**80**

Programme Educational Objectives	
PEO1	Pursue successful career in industry, academia, and entrepreneurial ventures in the domain of VLSI Design and Embedded Systems
PEO2	Identify relevant tools & apply appropriate knowledge to solve real time problems
PEO3	Engage in their profession with social awareness and responsibility
Programme Outcomes	
PO1	An ability to independently carry out research / investigation and development work to solve practical problems
PO2	An ability to write and present a substantial technical report / document
PO3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
PO4	An ability to function, manage and lead multidisciplinary teams
PO5	Acquire competency in the area of VLSI Design
PO6	Acquire competency in the area of Embedded Systems
Programme Specific Outcomes	
PSO1	Demonstrate an ability to apply knowledge of VLSI Design, Verification and Testing to solve practical problems
PSO2	Analyse real-world problems and design suitable embedded system solutions

NITTE (Deemed to be University) | NMAM INSTITUTE OF TECHNOLOGY

Established under Section 3 of UGC Act 1956 **Off-Campus Centre, Nitte - 574 110, Karkala**

Accredited with 'A+' Grade by NAAC

M.Tech. (VDE): Scheme of Teaching and Examinations 2022-24

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2022 - 23)

1st Year Scheme

I SEMESTER												
Sl. No	Course Type	Course Code	Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Lecture	Tutorial	Practical/ Drawing	Duration in Hours	CIEMarks	SEEMarks	Total Marks	
					L	T	P					
1	PCC	22VDE101	Digital VLSI Design	EC	4	0	0	3	**50**	**50**	**100**	**4**
2	PCC	22VDE102	Embedded System Design	EC	4	0	0	3	**50**	**50**	**100**	**4**
3	RETP	22VDE103	Research Experience Through Practice –I	EC	Four contact hours /week for carrying out Research and Interaction between the faculty and students			-	**100**	**0**	**100**	**2**
4	PCC	22VDE104	Digital VLSI Design Lab	EC	**0**	**0**	**2**	**3**	**50**	**50**	**100**	**1**
5	PCC	22VDE105	Embedded System Design Lab	EC	**0**	**0**	**2**	**3**	**50**	**50**	**100**	**1**
6	PEC	22VDE11X	Elective – I	EC	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**3**
7	PEC	22VDE12X	Elective – II	EC	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**3**
8	PEC	22VDE13X	Elective – III	EC	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**3**
9	AUDIT	22VDEAU1X	Audit Course-I	EC	**2**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
				Total	**19**	**0**	**4**	**21**	**450**	**350**	**800**	**21**

II SEMESTER												
Sl. No	**Course Type**	**Course Code**	**Course Title**	**Teaching Department**	**Teaching Hours /Week**			**Examination**				**Credits**
					Lecture	**Tutorial**	**Practical/ Drawing**	**Duration in Hours**	**CIE Marks**	**SEE Marks**	**Total Marks**	
					L	**T**	**P**					
1	PCC	22VDE201	Analog VLSI Design	EC	**4**	**0**	**0**	**3**	**50**	**50**	**100**	**4**
2	PCC	22VDE202	Real-time Operating Systems	EC	**4**	**0**	**0**	**3**	**50**	**50**	**100**	**4**
3	RETP	22VDE203	Research Experience Through Practice –II	EC	Four contact hours /week for carrying out Research and Interaction between the faculty and students			**-**	**100**	**0**	**100**	**2**
4	PCC	22VDE204	Analog VLSI Design Lab	EC	**0**	**0**	**2**	**3**	**50**	**50**	**100**	**1**
5	PCC	22VDE205	Real-time Operating Systems Lab	EC	**0**	**0**	**2**	**3**	**50**	**50**	**100**	**1**
	PEC	22VDE21X	Elective – IV	EC	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**3**
6	PEC	22VDE22X	Elective – V	EC	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**3**
7	PEC	22VDE23X	Elective – VI	EC	**3**	**0**	**0**	**3**	**50**	**50**	**100**	**3**
8	AUDIT	22VDEAU2X	Audit Course-II	EC	**2**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
				Total	**19**	**0**	**4**	**21**	**450**	**350**	**800**	**21**

Note: PCC: Professional Core Course, PEC: Professional Elective Course, AUDIT (AU): Non-credit Audit course, RETP: Research Experience Through Practice.
L –Lecture, T – Tutorial, P- Practical/ Drawing, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

2nd Year Scheme

III SEMESTER												
Sl. No	**Course Type**	**Course Code**	**Course Title**	**Teaching Department**	**Teaching Hours /Week**			**Examination**				**Credits**
					Lecture	**Tutorial**	**Practical/ Drawing**	**Duration in Hours**	**CIEMarks**	**SEEMarks**	**Total Marks**	
					L	**T**	**P**					
1	UCC	22VDE 301	Industry Internship/ Research Internship/Mini Project	EC	8 Weeks Full Time [40-45 Hrs/week]			3	100	0	100	8
2	UCC	22VDE 302	Seminar on Special Topic	EC	0	0	2	3	100	0	100	2
3	UCC	22VDE 303	Project Part -1	EC	12 Weeks Full Time Minimum 30 Hrs/week]			3	200	0	200	8
				Total	**0**	**0**	**2**	**9**	**400**	**0**	**400**	**18**
Note: L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.												
Internship: CIE Evaluation is for 100 Marks where 50 Marks is for Report and 50 Marks for the Presentation												
Project Part-1: CIE Evaluation is for 200 Marks where 100 Marks is for Report and 100 Marks for the Presentation												

IV SEMESTER

Sl. No	Course Type	Course Code	Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Lecture	Tutorial	Practical/ Drawing	Duration in Hours	CIEMarks	SEEMarks	Total Marks	
					L	T	P					
1	UCC	22VDE401	Project Part -2	EC	22 Weeks Full Time [36 Hrs/week]			**3**	**200**	**200**	**400**	**20**
				Total	**0**	**0**	**0**	**3**	**200**	**200**	**400**	**20**

Note: L –Lecture, T – Tutorial, P- Practical/ Drawing, S – Self Study Component, CIE: Continuous Internal Evaluation, SEE: Semester End Examination.

Project Part-2: CIE Evaluation is for 200 Marks having Project Progress Evaluation (PPE)-1 and PPE-2 each for 100 Marks.

NITTE (Deemed to be University) | NMAM INSTITUTE OF TECHNOLOGY

Established under Section 3 of UGC Act 1956 **Off-Campus Centre, Nitte - 574 110, Karkala**

Accredited with 'A+' Grade by NAAC

M.Tech. (VDE): Scheme of Teaching and Examinations 2022-24

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)

(Effective from the academic year 2022 - 23)

List of Domain Specific Skill Development Audit Course (AUDIT)	
Course Code	**Course Title**
22VDEAU11	Growth of Thin Films
22VDEAU21	LabVIEW

List of Electives [PEC]			
Elective – I		**Elective - II**	
Code	**Course Title**	**Code**	**Course Title**
22VDE111	Embedded System Programming	22VDE121	Advanced Digital System Design
22VDE112	VLSI Design Verification	22VDE122	Embedded Systems for Biomedical Applications
22VDE113	Multicore Processor and Systems	22VDE123	Low Power VLSI Design
Elective – III		**Elective - IV**	
Code	**Course Title**	**Code**	**Course Title**
22VDE131	Embedded Systems for Automotive Applications	22VDE211	Design for IoT and Cloud Computing
22VDE132	Embedded Systems in Robotics	22VDE212	MEMS and IC Integration
22VDE133	SoC Design	22VDE213	Synthesis and Optimization Digital Circuits
Elective – V		**Elective – VI**	
Code	**Course Title**	**Code**	**Course Title**
22VDE221	DSP Algorithms and Architecture	22VDE231**	Digital Control in Switched Mode Power Converters & FPGA-Based Prototyping
22VDE222	Embedded Controller Programming for Real Time Systems	22VDE232	Distributed Computing
22VDE223*	System Verilog for Verification and Testing	22VDE233	Scripting Languages for VLSI

* 22VDE223 is offered in association with P&C Tech

** Elective course 22VDE231 may be registered under NPTEL

DIGITAL VLSI DESIGN

Course Code:	**22VDE101**	**Course Type**	**PCC**
Teaching Hours/Week (L: T: P)	**4:0:0**	**Credits**	**04**
Total Teaching Hours	**50+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To analyze the MOS system under equilibrium, under bias and analyse current-voltage characteristic of MOSFET, analyze the critical voltages in the inverter static characteristics.
2.	To model interconnect delay and to estimate power dissipation in CMOS inverters.
3.	To analyze the temporary charge storage concept in dynamic logic circuits and salient features of BiCMOS circuits.
4.	To design data path arithmetic blocks.
5.	Understand the need for I/O circuits, design clock generation and distribution circuits and understand the issues in design for manufacturability.

UNIT-I

MOS Transistor and MOS Inverter Static Characteristics	**10 Hours**

The Metal Oxide Semiconductor (MOS) Structure, the MOS System under External bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling.

MOS inverter with resistive-Load Inverter, Inverter with n-Type

MOSFET load.

UNIT-II

CMOS Inverter Static Characteristics	**10 Hours**

MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time

definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of

Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

UNIT-III

Dynamic Logic Circuits and BiCMOS Logic Circuits	**10 Hours**

Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.

Introduction, Basic BiCMOS Circuits: Static Behavior.

UNIT-IV

CMOS Datapath Design	**10 Hours**

Introduction, Data path operators: Addition/subtraction: Single bit adders, Bit parallel adder, Bit-serial adders, Carry-save addition and pipelining, transmission gate adder, parity generators, Comparators,

Zero/One Detectors, Multiplication: Array Multiplier, carry-save multiplier, Shifter: Barrel Shifter, Logarithmic Shifter.

UNIT-V

Chip Input and Output (I/O) Circuits	**10 Hours**

Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.

Design for Manufacturability: Introduction, Process Variations, Basic Concepts and Definitions.

Course Outcomes: At the end of the course student will be able to

1.	Analyse the MOS system under bias, MOSFET current-voltage characteristics and estimate MOS Inverter noise margins.
2.	Design CMOS inverter for the given noise margin, DC and transient characteristics and also model the interconnect delays.
3.	Analyse dynamic logic circuits and BiCMOS circuits.
4.	Design data path arithmetic blocks.
5.	Design level shifter circuits, analyse I/O circuits, generate on-chip and off-chip clock, clock distribution networks and analyse the effect of random fluctuations in fabrication process, power supply voltage, operating temperature on the circuit performance.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE101.1	2	1	1	-	3	-	2	-
22VD E101.2	2	1		-	3	-	2	-
22VDE1 01.3	2	1	1	-	3	-	2	-
22VDE101.4	3	1	1	-	3	-	2	-
22VDE101.5	2	1	1	-	3	-	2	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Sung Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill, 3rd Edition, 2003.
2.	Neil Weste and K. Eshraghian, “Principles of CMOS VLSI Design: A System Perspective”, Pearson Education (Asia) Pvt. Ltd., 2nd Edition, 2000.
3.	Wayne Wolf, “Modern VLSI design: System on Silicon”, Pearson Education, Second Edition, 1998.
4.	Douglas A Pucknell & Kamran Eshraghian, “Basic VLSI Design”, PHI 3rd Edition (original Edition – 1994).

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/117106092

EMBEDDED SYSTEM DESIGN

Course Code:	**22VDE102**	**Course Type**	**PCC**
Teaching Hours/Week (L: T: P)	**4:0:0**	**Credits**	**04**
Total Teaching Hours	**50+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To understand the concept of embedded systems, physical world logic signal levels, basic latch, flip-flop types and sequential circuits.
2.	To illustrate the various techniques for the software modeling of a system.
3.	To understand the major phases of the development process for embedded systems.
4.	To analyze the requirement of a test strategy, capabilities and limitations of the equipment utilized to execute the strategy.
5.	To design embedded systems with VxWorks and MicroC Real Time Operating Systems.

UNIT-I

Introduction to Embedded Systems	**10 Hours**

Introduction to Embedded Systems- Hardware side: What is an embedded system, Building an embedded system, Register transfer language, A look at real-world gates-part I: signal levels, Part II: Time, Part III: The legacy of early physicists, Logic circuits and parasitic components, Testing combinational circuits, Modeling, simulation and tools, Structural faults, Functional faults, Practical considerations- Part I: timing in latches and flip-flops, Part II: Clocks and clock distribution, Testing sequential circuits.

UNIT-II

Introduction to Software Modelling	**08 Hours**

UML diagrams, use cases, Class diagrams, Dynamic modeling with UML, Interaction diagrams, Sequence diagrams, Fork and Join, Branch and Merge, Activity diagram, State chart diagram, Dynamic modeling with structured design methods.

UNIT-III

Embedded Systems Design and Development	**10 Hours**

Introduction, System design and development, Life cycle models, Problem solving: 5 steps to design, the design process, Identifying the requirement, Formulating the requirements specification, The system design specification, System specifications versus system requirements, Partitioning and decomposing a system, Functional design, Architectural design, Functional model versus architectural model, Prototyping.

UNIT-IV

Hardware Test and Debug	**10 Hours**

Hardware Test and Debug: Formalizing the plan, Executing the plan, Applying the strategy: Egoless design, Design reviews, Module debug and test, The first steps, Debugging and testing, Testing and debugging combinational logic, Path sensitizing, Masking and untestable faults, , Single variable- multiple paths, Bridge

faults, Debugging- sequential logic, Scan design testing, Boundary scan testing, Memories and memory systems, Applying the strategy: Subsystem and system test, Testing for our customer, Self-test.

UNIT-V

Embedded System Design with VxWorks	**12 Hours**

Operating system basics, Types of operating systems, Introduction to VxWorks, Task creation and management, Task scheduling, Kernel services, Inter-task communication, Task synchronization and Mutual exclusion, Interrupt handling, Watchdog for task execution monitoring, Timing and reference, VxWorks development environment, Introduction to MicroC/OS-II.

Course Outcomes: At the end of the course student will be able to

1.	Demonstrate the modeling of parasitic components and their effects on digital circuit and analyze the common faults in combinational and sequential circuits.
2.	Discuss the Unified Modeling Language (UML), analyze the static and dynamic modeling diagrams in UML.
3.	Illustrate product life cycle, five steps in design, life cycle models, and differentiate between functional and architectural models of a system.
4.	Discuss the need for planning, specifications, test procedures, and analyze the common faults in combinational and sequential circuitry.
5.	Discuss the types of operating systems; illustrate the implementations of the multitasking strategy, inter-task communication and synchronization for VxWorks and MicroC/OS-II.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE102.1	2	1	1	-	-	3	-	2
22VDE102.2	2	1	1	-	-	3	-	2
22VDE102.3	2	1	1	-		3	-	2
22VDE102 4	3	1	1	-	-	3	-	2
22 VDE102.5	2	1	1	-	-	3	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	James K. Peckol, “Embedded Systems - A Contemporary Design Tool”, John Wiley, 2008.
2.	Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2009.

E Books / MOOCs/ NPTEL

1.	https://onlinecourses.nptel.ac.in/noc20_ee98/preview
2.	https://onlinecourses.nptel.ac.in/noc22_cs46/preview

RESEARCH EXPERIENCE THROUGH PRACTICE -1

Course Code:	**22VDE103**	**Course Type**	**RETP**
Teaching Hours/Week (L: T: P)	**0:0:4**	**Credits**	**2**
Total Teaching Hours	**0+0+52**	**CIE**	**100**

Teaching Department: Any

Course Objectives: The research purposes are

1. To foresee future problems through pursuit of truth as a "global centre of excellence for intellectual creativity".
2. To respond to current social demands, and to contribute to the creation and development of scientific technologies with the aim of realizing an affluent society and natural environment for humanity.
3. At the same time, the course aims to create excellent educational resources and an excellent educational environment through frontline researches
4. To Understand professional writing and communication contexts and genres, analyzing quantifiable data discovered by researching, and constructing finished professional workplace documents.

Individual PG Students are to be allotted to the individual faculty members based on student's area of research interest, specialization of faculty members in the beginning of the first semester.

MODULE -1

Defining the research problem – Selecting the problem – Necessity of defining the problem -Techniques involved in defining the problem – Importance of literature review in defining a problem – Survey of literature – Primary and secondary sources – Reviews, treatise, monographs patents – web as a source – searching the web – Identifying gap areas from literature review – Development of working hypothesis, systematic way of conducting research, write a review / research paper, research proposal, preparation of research report.

MODULE-2

- Introduction various simulation tools related to VLSI and embedded systems.
- Use of software tools (MATLAB-Simulink, Cadence).
- Introduction to typesetting tool (Latex).
- At the end of the course students should submit a research proposal and should present the idea.

The Research proposal report prepared based on the work carried out by the PG Student is evaluated for 50 marks and 20 minutes presentation on the research work carried out will be evaluated for 50 marks jointly by the examiners.

Course Outcomes: At the end of the course student will be able to

1.	Identify and define the problem statement based on the literature reviewed.
2.	Formulate the objectives specific to the defined problem statement.
3.	Develop the methodology for achieving the objectives.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / ↓ Course Outcomes	1	2	3	4	5	6	PSO↓ 1	PSO↓ 2
22VDE103.1	3	3	2	-	1	1	1	1
22VDE103.2	3	3	2	-	1	1	1	1
22VDE103.3	3	3	2	-	1	1	1	

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Gina Wisker, "The Undergraduate Research Hand book", 2018.

E Books / MOOCs/ NPTEL

1.	https://www.classcentral.com/course/swayam-research-methodology-17760

DIGITAL VLSI DESIGN LAB

Course Code:	**22VDE104**	**Course Type:**	**PCC Lab**
Teaching Hours/Week (L: T: P)	**0:0:2**	**Credits:**	**01**
Total Teaching Hours:	**0+0+26**	**CIE + SEE Marks:**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To design CMOS inverter, adder and dynamic CMOS circuit for the given specifications.
2.	To perform simulations using available tool.

List of Experiments

Tool: CADENCE/SYNOPYS/MENTOR GRAPHICS.

1.	V-I characteristics of NMOSFET and determine MOSFET parameters.
2.	Design a CMOS Inverter for the desired mid-point voltage, analyse of the effect of MOSFET sizing on the inverter midpoint voltage.
3.	Schematic simulation of area efficient full adder.
4.	Design and simulation of a CMOS inverter for given switching specifications.
5.	Design and simulation of dynamic CMOS circuits
6.	Mini project.

Course Outcomes: At the end of the course student will be able to

1.	Design and simulate an inverter for the given DC and switching characteristics, an area efficient adder and dynamic CMOS circuit for the desired logic function.
2.	Design and implement a digital block.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE104.1	2	2	2	-	3	-	2	-
22VDE104.2	2	2	2	-	3	-	2	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Sung Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw- Hill, 3rd Edition, 2003.
2.	Neil Weste and K. Eshraghian, "Principles of CMOS VLSI Design: A System Perspective", Pearson Education (Asia) Pvt. Ltd., 2nd Edition, 2000.

E Resources

1.	http://www.eecs.umich.edu/courses/eecs522/w09/public/CadenceTutorial1W09.pdf

EMBEDDED SYSTEM DESIGN LAB

Course Code:	**22VDE105**	**Course Type:**	**PCC Lab**
Teaching Hours/Week (L: T: P:)	**0:0:2**	**Credits:**	**01**
Total Teaching Hours:	**0+0+26**	**CIE + SEE Marks:**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	Students should be able to develop the ability to design microcomputer-based embedded systems, which allows students to learn microcomputer interfacing from both a hardware and software perspective.

List of Experiments

1.	Write a C code to interface input device (Keyboard), with output devices (seven segment LEDs and free running LEDs) and display the contents of the key pressed on the output.
2.	Design a low pass FIR Filter using Simulink block sets.
3.	Verilog/VHDL File Processing (Reading a file and storing data in a file).
4.	Verilog/ VHDL LCD Display (Scrolling blinking etc.).

Course Outcomes: At the end of the course student will be able to

1.	Design an embedded System.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE105.1	2	2	2	-	-	3	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited.
2.	James K. Peckol, "Embedded Systems - A Contemporary Design Tool", John Wiley.

E Resources

1.	https://nptel.ac.in/courses/108102169
2.	https://onlinecourses.nptel.ac.in/noc22_cs46

EMBEDDED SYSTEMS PROGRAMMING

Course Code:	**22VDE111**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To understand Operating System Fundamentals
2.	To learn Embedded C
3.	To learn data structures and analyse examples

UNIT-I

Introduction	**15 Hours**

Introduction – Issues in Real Time Computing – Structure of a Real Time System – Task classes – Performance Measures for Real Time Systems – Estimating Program Run Times – Task, Assignment and Scheduling – Classical uniprocessor scheduling algorithms – Uniprocessor scheduling of IRIS tasks – Task assignment – Mode changes and Fault Tolerant Scheduling. Operating System Fundamentals, General and Unix OS architecture Embedded Linux.

UNIT-II

Embedded C Programming	**16 Hours**

Review of data types –scalar types-Primitive Types-Enumerated types-sub ranges Structure types character strings –arrays- Functions introduction to Embedded C- Introduction, Data types Bit manipulation, Interfacing C with Assembly. Embedded programming issues - Re-entrancy, Portability, Optimizing and testing embedded C programs.

UNIT-III

Applications Using Data Structures	**09 Hours**

Linear data structures– Stacks and Queues Implementation of stacks and Queues- Linked List - Implementation of linked list, Sorting, Searching, Insertion and Deletion, Nonlinear structures.

Course Outcomes: At the end of the course student will be able to

1.	Understand and analyse the issues of Real Time Computing
2.	Understand the Operating System Fundamentals
3.	Understand the basics of EMBEDDED C
4.	Develop programming skills in embedded systems for various applications
5.	Design various applications using data structures

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22 VDE111.1	2	1	1	-	-	3	-	2
22VDE 111.2	2	1	1	-	-	3	-	2
22VDE111.3	2	1	1	-	-	3	-	2
22VDE111.4	2	1	1	-	-	3	-	2
22VDE111.5	3	2	2	-	-	3	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Jones, M Tim, "GNU/Linux application programming", Dreamtech press, New Delhi
2.	E Prasad K.V.K.K, "Embedded / Real-Time Systems: concepts, Design and Programming—The Ultimate Reference", Dream Tech Press, New Delhi.
3.	Samiran Chattopadhyay, Debarata Ghosh Dastidar, Matangini Chattopadhyay, "Data structures Through 'C' Language", DOEACC Society.
4.	Stevens, W Richard, PH, "Unix Network Programming", New Jersey ACC.NO: B126496.

E Books / MOOCs/ NPTEL

1.	https://www.digimat.in/nptel/courses/video/106105193/L01.html
2.	https://www.youtube.com/watch?v=y9RAhEfLfJs
3.	https://onlinecourses.nptel.ac.in/noc20_ee98/preview

VLSI DESIGN VERIFICATION

Course Code:	**22VDE112**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	The role of testing and verification in VLSI Development Process.
2.	An understanding on the functional and block level verification techniques in VLSI development process.
3.	The different timing constraints with respect to VLSI Design Process.
4.	The physical design verification techniques in VLSI development process.
5.	The testing process and the testing equipment.

Prerequisite: Should have undergone an Undergraduate course on VLSI Design or equivalent

UNIT-I

Introduction to Verification in VLSI Development process	**15 Hours**

Introduction: VLSI development process, role of testing and verification, verification methodology, Types of Design Verification - Functional Verification, Simulation Emulation Testing and verification: how to test chips? VLSI Technology Trends Affecting Testing.

Block-level Verification. Functional Verification through simulation. White box, black box and grey box testing. Verilog/VHDL test bench for functional verification

UNIT-II

Static Timing Analysis	**15 Hours**

Static Timing Verification. Concept of static timing analysis. Timing constraints, timing models, critical path analysis, false paths. Physical Design Verification. Layout rule checks and electrical rule checks. Parasitic extraction.

Logic and fault simulation: Modelling circuit for simulation, event driven simulation, serial fault simulation

UNIT-III

Testing Equipment	**10 Hours**

ATPG for combinational circuit, BIST. Test equipment, electrical parametric testing. Design for testability and scan, scan cell design.

Course Outcomes: At the end of the course student will be able to

1.	Explain the role of testing and verification in VLSI Development Process.

2.	Discuss the functional and block level verification techniques in VLSI development process.
3.	Discuss the different timing constraints with respect to VLSI Design Process; Determine the set-up time, hold time, propagation delay, maximum and minimum clock period and clock frequency for a given logic circuit.
4.	Explain the physical design verification techniques in VLSI development process.
5.	Explain Automatic Test Pattern Generation and BIST architecture, Explain electrical parametric tests, DFT and Scan design in VLSI testing process.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Cour e Outcomes							1	2
22VDE112.1	1	2	3	-	3	-	3	-
22VDE112. 2	1	2	3	-	3	-	3	
22VDE112.3	1	2	3	-	3	-	3	-
22VDE112.4	1	2	3	-	3	-	3	-
22VDE112.5	1	2	3	-	3	-	3	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	M. Bushnell, Vishwani Agrawal, "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002
2.	Prakash Rashinkar, Peter Paterson and Leena Singh "System – on – a - Chip Verification – Methodology and Techniques", Kluwer Academic Publishers, 2001.
3.	Laung-Terng wang, Cheng-Wen wu & Xiaoping Wen, "VLSI Test Principles and Architectures- Design for Testability", Morgan Kaufmann, 2006.
4.	S. Minato "Binary Decision Diagram and Applications for VLSI CAD", Kulwer Academic Pub. November 1996.

E Books / MOOCs/ NPTEL

1.	"An Excellent Source for Instructors for Formal Verification Techniques" (website developed by) Prof. V. Narayanan, Penn state University, USA, http://www.cse.psu.edu/~vijay/verify/instuctors.html

MULTICORE PROCESSOR AND SYSTEMS

Course Code:	**22VDE113**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To develop knowledge on the Issues involved in the multi-core architectures.
2.	To enrich skills in using Multi-core Network-on-chip.
3.	To gain knowledge about the low power reconfigurable cores.

UNIT-I

Instruction Level and Thread Level Parallelism	**15 Hours**

Fundamentals of Computer Design-Instruction- Level Parallelism: Concepts and Challenge-Basic Compiler. Techniques- Branch Prediction- Dynamic Scheduling- Hardware based Speculation- Multiple Issue and Static Scheduling-Intel Pentium 4 Architecture- Limitations on Instruction- Level Parallelism.

Multiprocessors and Thread-Level Parallelism: Symmetric Shared-Memory Architectures- Performance- Distributed Shared Memory and Directory-Based Coherence- Synchronization- Models of Memory Consistency- Crosscutting Issues- Sun T1 Multiprocessor - Motivation for Concurrency in Software- Parallel Computing Platforms.

UNIT-II

Threading and Message-Passing Programming	**15 Hours**

System Overview of Threading- Fundamental Concepts of Parallel Programming - Parallel Programming Patterns- Error Diffusion- Threading and Parallel Programming Constructs- Threading APIs for Microsoft .NET Framework.

Message-Passing Programming: The message-passing model – the message-passing interface – MPI standard – basic concepts of MPI- Point to Point communication– collective communication– Communicators- Topologies- Case studies: the sieve of Eratosthenes.

UNIT-III

Multicore Systems On-Chip and Low Power Reconfigurable Cores	**10 Hours**

MCSoCs Design Problems – SoC typical architecture- Application specific MCSoC design method, Queue Core architecture, QC2 Core -Reconfigurable Multicore: Power Aware technological level optimizations - Power Aware system design optimizations. Network-on-Chip – Topology, Routing.

Course Outcomes: At the end of the course student will be able to

1.	Achieve Parallelism using Instruction Level Parallelism
2.	Demonstrate the concepts of Thread Level Parallelism
3.	Develop programs using threading

4.	Write programs using MPI
5.	Develop low power reconfigurable multi-core architectures

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE113.1	3	2	1	-	1	-	1	2
22VDE113.2	3	3	-	-	2	1	-	1
22VDE113.3	3	-	-	1	-	1	-	1
22VDE113.4	3	-	-	-	-	1	-	1
22VDE113.5	3	-	-	-	-	3	2	1

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Shameem Akhter and Jason Roberts, "Multicore Programming", BPB Publications, First Edition, 2010.
2.	Ben Abadallah Abderazek, "Multicore Systems On-chip: Practical Software/Hardware Design", Atlantis Press, Second Edition, 2010.
3.	Michael J Quinn, "Parallel programming in C with MPI and Open MP", Tata McGraw Hill, First Edition, 2003.
4.	John L. Hennessey and David A. Patterson, "Computer architecture – A quantitative approach", Morgan Kaufmann/Elsevier Publishers, Fifth Edition, 2011.
5.	David E. Culler and Jaswinder Pal Singh, "Parallel computing architecture: A hardware/software approach", Morgan Kaufmann/Elsevier Publishers, First Edition, 1999.

E Books / MOOCs/ NPTEL

1.	http://www.csa.com/discoveryguides/multicore/review.pdf
2.	http://www.mpi-forum.org/docs/

ADVANCED DIGITAL SYSTEM DESIGN

Course Code:	**22VDE121**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To introduce Finite State Machines.
2.	To understand the difference between a Mealy machine and a Moore machine.
3.	To design sequential circuits by specifying suitable set of state assignments for a state table.
4.	To introduce the basic concepts of Fault detection.
5.	To understand different methods of test generation for combinational and sequential circuits.

Prerequisite: Should have undergone an Undergraduate course on Digital System design or equivalent

UNIT-I

Synchronous Sequential Circuits	**15 Hours**

Synchronous Sequential Circuits: Finite State Model- definitions, Synthesis of synchronous sequential Circuits, State Equivalence and Machine Minimization, Simplification of incompletely specified Machines.

UNIT-II

Asynchronous Sequential Circuits	**10 Hours**

Introduction, Flow Table, Reduction of Primitive Flow tables, Races and Cycles, Critical Race-free State Assignment, Excitation and Output Functions, Hazards.

UNIT-III

Fault Detection in Logic Circuits	**15 Hours**

Basic concepts of Fault detection; Test Generation for Combinational Logic: Fault Matrix, Path Sensitization, D-Algorithm, PODEM, Delay Fault Detection; Testing of Sequential Circuits: Checking experiments, Test generation using circuit structure and state table.

Course Outcomes: At the end of the course student will be able to

1.	Write the next-state equations, derive the state graph or state table and using the state graph, determine the state & output sequence for a specified input sequence for a synchronous sequential circuit.

2.	Design a synchronous sequential circuit, using gates and flip-flops, by Specifying a suitable set of state assignments eliminating equivalent states with respect to the minimizing the cost of realizing the circuit.
3.	Derive the excitation and output equations for an asynchronous sequential circuit by constructing the Flow table and performing a race-free state assignment; Implement a hazard-free realization for a given logic circuit or switching function.
4.	Derive a Minimal Test Pattern to detect stuck-at faults in Combinational circuits.
5.	Design a checking experiment to test sequential circuit.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE121.1	1	-	3	-	3	-	3	-
22VDE121.2	1	-	3	-	3	-	3	-
22VDE121.3	1	-	3	-	3	-	3	-
22VDE121.4	1	-	3	-	3	-	3	-
22VDE121.5	1	-	3	-	3	-	3	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Z. Kohavi and N. Jha, "Switching and Finite Automata theory", 3rd Edition, Cambridge University Press, 2010.
2.	Parag K. Lala, "An Introduction to Logic Circuit Testing", Synthesis Lectures on Digital Circuits and Systems, 2008, Vol. 3, No. 1, Pages 1-100 (https://doi.org/10.2200/S00149ED1V01Y200808DCS017).
3.	Parag K. Lala, "Principles of Modern Digital Design", Wiley Inter-science, 2007.
4.	Charles H. Roth, Jr. and Larry L. Kinney, "Fundamentals of Logic Design", 7th Edition, Cengage Learning, 2014.
5.	M Morris Mano, Michael Ciletti, "Digital Design: With an introduction to the Verilog HDL", Pearson, 5th Edition, 2013.

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/108106177

EMBEDDED SYSTEMS FOR BIOMEDICAL APPLICATIONS

Course Code:	**22VDE122**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To understand the concepts of embedded operating systems
2.	To study PIC microcontrollers and embedded system evolution trends
3.	To learn various Embedded Database Applications

UNIT-I

Embedded Operating Systems	**15 Hours**

Definition and Classification – Overview of Processors and hardware units in an embedded system – Software embedded into the system – Exemplary Embedded Systems – Embedded Systems on a Chip (SoC) and the use of VLSI designed circuits - Embedded Hardware Architecture, Communication Interface Standards, Embedded System Development Process, Embedded Operating systems, Types of Embedded Operating systems.

Intel MCS51 Architecture – Derivatives - Special Function Registers (SFR), I/O pins, ports and circuits, Instruction set, Addressing Modes, Assembly Language Programming, Timer and Counter Programming, Serial Communication, Connection to RS 232, Interrupts Programming, External Memory interfacing.

UNIT-II

PIC Microcontrollers	**15 Hours**

PIC Microcontroller - Introduction, CPU architecture, registers, instruction sets addressing modes Loop timing, timers, Interrupts, Interrupt timing, I/o Expansion, I 2C Bus Operation Serial EEPROM, Analog to digital converter, UART-Baud Rate-Data Handling-Initialization.

Embedded system evolution trends. Round - Robin, robin with Interrupts, function-One-Scheduling Architecture, Algorithms. Introduction to-assembler-compiler-cross compilers and Integrated Development Environment (IDE). Object Oriented Interfacing, Recursion, Debugging strategies, Simulators. Task and Task States, tasks and data, semaphores and shared Data Operating system Services-Message queues-Timer Function-Events-Memory Management, Interrupt Routines in an RTOS.

UNIT-III

Applications	**10 Hours**

Real-Time Embedded Software Development, Sending a Message over a Serial Link, Simulation of a Process Control System, Controlling an Appliance from the RT Linux System, Embedded Database Applications, Embedded medical applications: Ophthalmology - Glaucoma screening device, Medical Imaging Acquisition User Interface, Drug delivery systems, Patient monitoring Systems.

Course Outcomes: At the end of the course student will be able to

1.	Understand the concept of embedded system design and its application in different design and product, Programming for Embedded System Design. Understand architecture and functionalities of each block inside the processor.
2.	Get idea about working of processor and its application. Select appropriate microcontroller for design. Calculate memory requirement and other on-chip/off-chip peripheral requirement.
3.	Understand requirement of a project as well as inputs and outputs of the system. Make flowchart of different tasks and decisions.
4.	Understand multitasking environment and development tools. Design software for the target processor/controller.
5.	Interface peripherals with the board. Understand different communication protocols to make the system as a part of network.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE122.1	1	1	2	-	-	3	-	2
22VDE122.2	1	1	2	-	-	3	-	2
22VDE122.3	1	1	2	-	-	3	-	2
22VDE122.4	2	2	2	-	-	3	-	2
22VDE122.5	2	2	2	-	-	3	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Rajkamal, "Embedded Systems Architecture, Programming and Design", TATA McGraw-Hill, First reprint Oct. 2003.
2.	Tim Wilmshusrst, "Designing Embedded Systems with PIC", Newnes publishing, 2007.
3.	David E. Simon, "An Embedded Software Primer", Pearson Education Asia, First Indian Reprint 2000.

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/106105193

LOW POWER VLSI DESIGN

Course Code:	**22VDE123**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To understand the factors affecting the power in VLSI circuits.
2.	Understand the concepts and techniques of Low power VLSI.
3.	To develop a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction
4.	To obtain an understanding on the special and advanced techniques of low power design.

UNIT-I

Introduction to Sources of power dissipation	**15 Hours**

Sources of power dissipation on Digital Integrated circuits; Static, Dynamic and Short circuit components, Emerging Low power approaches- An overview, Physics of power dissipation in CMOS devices, Basic Principles of Low Power Design, Low power design Figure of Merits, Low Power VLSI Design: Limits, Device & Technology Impact on Low Power Electronics, Overview of power optimization at various levels.

UNIT-II

Power optimization at different abstraction levels	**15 Hours**

Logic Level and Circuit Level Optimization: Theoretical background – Calculation of Steady state probability- Transition probability -Conditional probability- Transition density- Estimation and optimization of Switching activity. Transistor variable re-ordering for power reduction- Low power library cell design (GDI)- Estimation of glitching power- leakage power optimization-Subthreshold logic design.

Algorithmic and Architecture Level Optimization: Pipelining and Parallel Processing approaches for low power design, Multiple supply voltage and Multiple threshold voltage designs for low power

UNIT-III

Special and Advanced low power techniques	**10 Hours**

Special Techniques: Power Reduction in clock networks, Low Power Bus, Low Power Techniques for SRAM.

Advanced Low Power Techniques: Adiabatic Computation, Pass Transistor Logic Synthesis

Software Design for Low Power: Sources of software power dissipation, Software Power Estimation, Software Power Optimizations.

Course Outcomes: At the end of the course student will be able to

1.	Explain the need for low power design in VLSI chips, sources of power dissipation in CMOS circuits and describe the device and technology impact on low power VLSI design.
2.	Explain the basic principle of low power design, its figure of merits, limits of Low Power VLSI design and to provide an overview of power optimization at various levels.
3.	Discuss the different power optimization techniques at logic and circuit level.
4.	Discuss the different power optimization techniques at algorithmic and architectural level.
5.	Discuss the different special and advanced techniques of low power design, discuss the software design for low power.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE123.1	1	2	2	-	3	-	3	-
22VDE123.2	1	2	2	-	3	-	3	-
22VDE123.3	1	2	2	-	3	-	3	-
22VDE123.4	1	2	2	-	3	-	3	-
22VDE123.5	1	2	2	-	3	-	3	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design”, Wiley, 2000.
2.	Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002.
3.	Rabaey, Pedram, “Low Power Design Methodologies”, Kluwer Academic, 1997.
4.	Anantha P. Chandrakasan & Robert W. Brodersen, “Low Power Digital CMOS Design” Kluwer Academic Publications, 1994.

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/106/105/106105034/

EMBEDDED SYSTEMS FOR AUTOMOTIVE APPLICATIONS

Course Code:	**22VDE131**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To introduce the vehicle Functional Domains and Embedded Systems.
2.	To understand the different Embedded Automotive protocols.
3.	To introduce the basic concepts of Functional Safety and Diagnostics.

Prerequisite: Should have undergone an Undergraduate level course on Embedded System or equivalent

UNIT-I

Automotive Fundamentals:	**09 Hours**

Vehicle Functional Domains and Their Requirements, Model Based Development of Automotive Embedded Systems, Automotive Description Languages.

UNIT-II

Embedded Automotive Protocols	**15 Hours**

FlexRay Protocol, Testing & Monitoring of FlexRay based Applications, CAN Protocol, Timing analysis of CAN-based Communication Systems.

UNIT-III

AUTOSAR & Functional Safety	**16 Hours**

AUTOSAR Basics, Software Components & Application Layer, Basic Software Layer, MCAL Layer, Services Layer, Diagnostics; Automotive Functional Safety Concepts: ISO26262 Definitions, why functional safety, Hazard and Risk Analysis, Safety Concepts.

Course Outcomes: At the end of the course student will be able to

1.	Describe the functions embedded in a vehicle, its division based on vehicular domains, and the development process involved.
2.	Explain the architecture and application of CAN based communication systems.
3.	Explain the architecture and application of FlexRay Protocol.
4.	Describe the layer architecture of AUTOSAR.

5.	Explain the concept of Failure mode analysis, Risk assessments as applicable to Automotive Safety.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE131.1	-	-	1	-	-	3	-	-
22VDE131.2	-	-	1	-	-	3	-	-
22VDE131.3	-	-	1	-	-	3	-	-
22VDE131.4	-	-	1	-	-	3	-	-
22VDE131.5	-	-	1	-	-	3	-	1

1: Low 2: Medium 3: High3

REFERENCE BOOKS:

1.	Nicolas Navet and Françoise Simonot-Lion, "Automotive Embedded Systems Handbook", CRC Press, 2009.
2.	Hans-Leo Ross, "Functional Safety for Road Vehicles New Challenges and Solutions for E-mobility and Automated Driving", Springer 2016.
3.	Miroslaw Staron, "Automotive Software Architectures an Introduction", 2nd Edition, 2021.

E Books / MOOCs/ NPTEL

1.	https://cse.buffalo.edu/~bina/cse321/fall2015/Automotive-embedded-systems.pdf
2.	Overview of Functional Safety Measures in AUTOSAR
3.	Microsoft PowerPoint - Shrikant (siliconindia.com)
4.	Automotive Embedded Systems Course | Online Course with Certification (easycourses.in)
5.	https://www.academia.edu/35270424/Kpit_autosar_handbook
6.	https://software-dl.ti.com/hercules/hercules_docs/latest/hercules/AutoSAR_MCAL/AutoSAR_MCAL.html
7.	https://www.autosar.org/fileadmin/user_upload/standards/classic/4-3/AUTOSAR_EXP_LayeredSoftwareArchitecture.pdf

EMBEDDED SYSTEMS IN ROBOTICS

Course Code:	**22VDE132**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To develop knowledge on the various hardware devices employed in robotics
2.	To gain knowledge in Robot movement
3.	To understand the Robot operating system and Robot programming

UNIT-I

Sensors and Actuators	**15 Hours**

Embedded Controllers, Interfaces, Operating System.

Sensors - Sensor Categories, Binary Sensor, Analog versus Digital Sensors, Shaft Encoder; A/D Converter, Position Sensitive Device; Compass, Gyroscope, Accelerometer, Inclinometer, Digital Camera.

Actuators - DC Motors, H-Bridge, Pulse Width Modulation, Stepper Motors, Servos.

Control - On-Off Control, PID Control, Velocity Control and Position Control.

UNIT-II

Industrial Robots and Trajectory Planning	**15 Hours**

Industrial Robots - Evolution of robotics, Robot anatomy, Design and control issues, Manipulation and Control.

Direct Kinematic Model - Denavit-Hartenberg Notation, Kinematic Relationship between adjacent links, Manipulator Transformation Matrix; Inverse Kinematic Model – Manipulator Workspace, Solvability, Solution techniques, Closed form solution.

UNIT-III

Robot motion and Programming	**10 Hours**

Mobile Robots, Concepts of Localization and path planning.

Autonomous robots and Introduction to Robot Operating System.

Course Outcomes: At the end of the course student will be able to

1.	Understand the importance of embedded systems and robotics in our daily life and identify different embedded devices.
2.	Identify different components of embedded systems and robotics.

3.	Design mechanical structure of a robot.
4.	Understand the robot configuration and sub-systems.
5.	Understand principle of robot programming.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Cours Out omes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE132.1	3	2	2	-	1	-	-	2
22VDE132.2	3	3	-	-	2	1	-	2
22VDE132.3	3	-	-	1	-	1	-	-
22VDE132.4	3	-	-	-	-	1	-	2
22VDE132.5	3	-	-	-	-	3	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Thomas Bräunl, "Embedded Robotics: Mobile Robot Design and Applications with Embedded Systems", Third Edition, Springer-Verlag Berlin Heidelberg, 2008.
2.	R.K.Mittal and I.J.Nagrath, "Robotics and Control", Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2003.
3.	John J. Craig, "Introduction to Robotics: Mechanics and Control", Third Edition, Pearson/Prentice Hall, 2005.
4.	AnisKoubaa, "Robot Operating System (ROS) The Complete Reference", First Volume, Springer, 2016.
5.	K.S. Fu, R.C. Gonzalez and C.S.G. Lee, "Robotics: Control, Sensing, Vision, and Intelligence", McGraw-Hill, New York, 1987.

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/108102045

SYSTEM ON CHIP (SOC) DESIGN

Course Code:	**22VDE133**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To Get an insight to the fundamentals and the general structure of System on chip and its goals.
2.	To Illustrates IP based design and design reuse.
3.	To understand MPSoCs.
4.	To learn the Energy-Aware Processor.

UNIT-I

Motivation for SoC Design	**15 Hours**

Review of Moore's law and CMOS scaling, benefits of system on chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System on Chip, and System in Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

UNIT-II

MPSoCs	**15 Hours**

What are MPSoCs ,Why MPSoCs, Challenges, Design Methodologies, Hardware Architectures

Techniques for Designing Energy-Aware MPSoCs: Energy-Aware Processor Design, Reducing Active Energy, Reducing Standby Energy, Energy-Aware Memory System Design, Reducing Active Energy, Reducing Standby Energy, Influence of Cache Architecture on Energy, Reducing Snoop Energy, Energy-Aware On-Chip Communication System Design, Bus Encoding for Low Power, Low Swing Signaling, Energy Considerations in Advanced Interconnects.

UNIT-III

SoC Design Flow	**10 Hours**

IP design, Set Top Box SOC, ASIC Design flow.

Verification: Types of design validation and verification. Formal verification, Assertion based verification,

Design for integration: More on VoIP SoC, hardware-software co-design flow, hardware-software co-design at system level.

1.	Recall the fundamentals of VLSI and classify SoC, SoB and SiP.

2.	Understand the different IP based design to apply in SoCs.
3.	Explain the typical peripherals in aMP SoC and Hardware Accelerators in a MPSoC.
4.	Summarize the energy aware systems.
5.	Illustrate the design flow and packaging related problems in the field of SoC.

Course Outcomes: At the end of the course student will be able to

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE133.1	1	2	3	-	3	-	3	-
22VDE133.2	1	2	3	-	3	-	3	-
22VDE133. 3	1	2	3	-	3	-	3	-
22VDE133.4	1	2	3	-	3	-	3	-
22VDE133.5	1	2	3	-	3	-	3	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.
2.	Henry Chang et al., "Surviving the SoC Revolution: A Guide to Platform-Based Design", Kluwer (Springer), 1999.
3.	Rao R. Tummala, Madhavan Swaminathan, "Introduction to System-on-Package (SOP) Miniaturization of the Entire System" Copyright, 2008.
4.	Prakash Rashinkar, Peter Paterson and Leena Singh, "System on a Chip Verification Methodology and Techniques", Kulwer Publishers, 2001.
5.	Ahmed Amine Jerraya and Wayne Wolf, "Multiprocessor Systems-on-Chips", Morgan Kaufmann Publishers is an imprint of Elsevier, 2005.

GROWTH OF THIN FILMS

Course Code:	**22VDEAU11**	**Course Type:**	**AUDIT**
Teaching Hours/Week (L: T: P)	**1:0:1**	**Credits:**	**-**
Total Teaching Hours:	**13+0+26**	**CIE + SEE Marks:**	**-**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To prepare appropriate molecular species
2.	To transport of molecular species to the substrate
3.	To characterize the developed films
4.	To analyse the developed films

List of Experiments

1.	Study of thin films
2.	Study of various thin film deposition techniques
3.	Study of Spray Pyrolysis Unit
4.	Identifying the suitable materials for deposition
5.	Preparation of molecular species
6.	Thin film Deposition on substrate
7.	Optimization of the thin films
8.	Study of various characterization technique
9.	Characterization of developed thin films
10.	Analysis based on Characterization

Course Outcomes: At the end of the course student will be able to

1.	Understand the difference between bulk and thin films
2.	Prepare a molecular species
3.	Transport of molecular species to the substrate

4.	Optimize the developed thin films
5.	Characterize the thin films and to analyze the results of characterization.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDEAU11 .1	1	1	1	1	1	1	2	1
22VDEAU11.2	1	1	1	1	1	1	2	1
22VDEAU11.3	1	1	1	1	1	1	2	1
22VDEAU11.4	3	2	2	2	2	1	3	1
22VDEAU11.5	3	3	3	3	2	1	2	1

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	M. Ohring, “Materials science of thin films”, Academic press, 2006.
2.	XZ.L.Wang, “Characterization of Nanostructure materials”.

E Resources

1.	https://nptel.ac.in/courses/113104075
2.	https://www.digimat.in/nptel/courses/video/113105099/L41.html
3.	https://nptel.ac.in/courses/113106034

ANALOG VLSI DESIGN

Course Code:	**22VDE201**	**Course Type**	**PCC**
Teaching Hours/Week (L: T: P)	**4:0:0**	**Credits**	**04**
Total Teaching Hours	**50+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To analyse the MOS current-voltage characteristics, the second order effects in MOS devices and model MOS devices.
2.	To analyse and design single stage MOSFET amplifiers.
3.	To analyse common mode and differential mode of operations in differential amplifiers and design current mirrors.
4.	Determine the frequency response of MOSFET amplifiers.
5.	To analyse the Op-amp circuit operation, different types of oscillators, PLL and DLL.

UNIT-I

Basic MOS Device Physics	**08 Hours**

General considerations, MOS I/V Characteristics, second order effects, MOS device models. MOS Device as a Capacitor**.**

UNIT-II

Single Stage Amplifier	**10 Hours**

CS stage with resistance load, diode connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascode stage, Folded cascode, choice of device models.

UNIT-III

Differential Amplifiers	**12 Hours**

Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell. Passive and active Current mirrors: Basic current mirrors, Cascode current mirrors, active current mirrors.

UNIT IV

Frequency Response of Amplifier	**10 Hours**

General considerations, Common source stage, source follower, Common gate stage. Noise in CS stage, CG stage, source follower.

UNIT V

Operational Amplifiers	**10 Hours**

One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compensation of two stage OP-Amp. Oscillators: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO. PLL: Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

Course Outcomes: At the end of the course student will be able to

1.	Explain MOSFET operation, characteristics, second order effects and device models
2.	Design and analyze single stage amplifiers using MOSFETs.
3.	Design and analyze differential amplifiers using MOSFETs and current mirrors.
4.	Analyze the high frequency behavior and noise in analog circuits using MOSFETs.
5.	Design and analyze op-amps using MOSFETs, Implement oscillators, VCO and PLL in CMOS technology.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE201.1	2	1	2	-	3	-	2	-
22VDE201.2	2	1	2	-	3	-	2	-
22VDE2 1 1.3	2	1	2	-	3	-	2	-
22VDE201.4	2	1	2	-	3	-	2	-
22VDE201.5	2	1	2	-	3	-	2	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH, 2007.
2.	R. Jacob Baker, Harry W. Li., David E. Boyce, “CMOS: Circuit Design, Layout and Simulation”, PHI, 2003.

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/108106105
2.	https://nptel.ac.in/courses/117101105

REAL TIME OPERATING SYSTEM

Course Code:	**22VDE202**	**Course Type**	**PCC**
Teaching Hours/Week (L: T: P)	**4:0:0**	**Credits**	**04**
Total Teaching Hours	**50+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	Get a brief introduction to the history of real-time operating systems, understand basic concepts of scheduling policies.
2.	Analyze Scheduling algorithms for better understanding the execution of real time services.
3.	Understand memory and I/O architectures of real-time systems for better design, understand software and hardware challenges faced by a real-time system service to meet deadlines.
4.	Get knowledge on embedded system components and debugging components.
5.	Understand performance tuning procedures to design better systems, analyze the high reliability and high availability designs.

UNIT-I

Introduction to Real-Time Systems	**10 Hours**

Introduction to Real-Time Embedded Systems: Brief history of Real-Time Systems, a Brief history of Embedded Systems, Real-Time services, and Real-Time standards.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts: Preemptive Fixed Priority Scheduling Policy, Real-Time OS, Thread Safe Reentrant Functions.

UNIT-II

Process Management	**10 Hours**

Preemptive Fixed-Priority Policy, Feasibility, Rate-Monotonic Least Upper Bound, Necessary and Sufficient Feasibility, Deadline-Monotonic Policy, Dynamic-Priority Policies.

UNIT-III

Resource Management	**10 Hours**

Resources: Worst-Case Execution Time, Intermediate IO, Execution Efficiency, IO Architecture.

Memory: Physical Hierarchy, Capacity and Allocation, Shared Memory, ECC Memory: Illustration using Hamming encoding, Flash File Systems.

Multiresource Services: Blocking, Deadlock and Livelock, Critical sections to Protect Shared Resources, Priority Inversion and its solutions.

Soft-Real-Time Services: Missed Deadlines, Quality of Service, Alternatives to Rate Monotonic Policy, Mixed Hard and Soft Real-Time Services

UNIT IV

Embedded System and Debugging Components	**12 Hours**

Embedded System Components: Hardware Components, Firmware Components, RTOS System Software, Software Application Components.

Debugging Components: Exceptions, Asserts, Checking Return Codes, Single-Step Debugging, Test Access Ports, Trace Ports, Power-On Self-Test and Diagnostics, Application-Level Debugging.

UNIT V

Performance, Availability and Reliability Design	**8 Hours**

Performance Tuning: Basic Concepts of Drill-Down Tuning, Hardware-Supported Profiling and Tracing, Building Performance Monitoring into Software, Path Length, Efficiency, and Calling Frequency, Fundamental Optimizations.

High Availability and Reliability Design: Reliability and Availability: Similarities and Differences, Reliability, Reliable Software, Available Software, Design Trade Offs, Hierarchical Applications for Fail-Safe Design.

Course Outcomes: At the end of the course student will be able to

1.	Understand the history and concepts of RTOS such as real-time services and standards. Describe the concepts of system resources such as utility, scheduling, and reentrant functions.
2.	Examine the operational principle of different scheduling algorithms and their characteristics.
3.	Analyze the concepts of I/O and Memory resources, examine the basic problems faced by multi-resource services, and solve challenges faced by soft real time services.
4.	Recognize and resolve software and hardware challenges faced by real-time systems to meet service deadlines and get awareness on embedded system components and debugging components.
5.	Evaluate basic performance tuning procedures to design and build improved systems and explore high reliability and high availability designs.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE202.1	1	1	2	-	-	3	-	3
22VDE202.2	2	1	2	-	-	3	-	3
22VDE202.3	2	1	2	-	-	3	-	3
22VDE202.4	3	1	2	-	-	3	-	3
22VDE202.5	3	1	2	-	-	3	-	3

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Sam Siewert, John Pratt, “Real-Time Embedded Components and Systems with Linux and RTOS”, Mercury Learning and Information, 2015.
2.	C.M. Krishna, Kang G Shin, “Real Time Systems”, McGraw-Hill, 1997.
3.	Raj Kamal, “Embedded System- Architecture, programming and Design”, 2nd Edition, Tata McGraw-Hill Education Pvt. Ltd., 2008.
4.	Dreamtech Software Team, “Programming for Embedded Systems”, John Wiley, India Pvt. Ltd., 2008.
E Books / MOOCs/ NPTEL	
1.	https://nptel.ac.in/courses/106105036
2.	https://www.coursera.org/learn/real-time-systems#syllabus
3.	https://www.udemy.com/course/real-time-operating-system/

RESEARCH EXPERIENCE THROUGH PRACTICE -2

Course Code:	**22VDE203**	**Course Type**	**RETP**
Teaching Hours/Week (L: T: P)	**0:0:4**	**Credits**	**2**
Total Teaching Hours	**0+0+52**	**CIE**	**100**

Teaching Department: Electronics and Communication Engineering

Course Objectives: The research purposes are

1. To foresee future problems through pursuit of truth as a "global centre of excellence for intellectual creativity".
2. To respond to current social demands, and to contribute to the creation and development of scientific technologies with the aim of realizing an affluent society and natural environment for humanity.
3. At the same time, the course aims to create excellent educational resources and an excellent educational environment through frontline researches.
4. To Understand professional writing and communication contexts and genres, analyzing quantifiable data discovered by researching, and constructing finished professional workplace documents.

The students are expected to carry out Mathematical 77odelling/Design calculations/computer simulations/Preliminary experimentation/testing of the research problems identified during Research Experience through Practice-I carried out in the first semester.

At the end of the second semester, students are expected to submit a full research paper based on the Mathematical modelling/ Design calculations/computer simulations/Preliminary experimentation/testing carried out during second semester.

The research paper prepared based on the work carried out by the PG Student is evaluated for 50 marks and 20 minutes presentation on the research work carried out will be evaluated for 50marks jointly by the examiners.

Course Outcomes: At the end of the course student will be able to

1.	Create a model/prototype through fabrication, simulation, data analysis, Experimentation for the proposed problem.
2.	Analyse and validate the results obtained.
3.	Compose a technical paper as per the given format.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE203.1	3	3	2	-	1	1	1	1
22VDE203.2	3	3	2	-	1	1	1	1
22VDE203.3	3	3	2	-	1	1	1	1

1: Low 2: Medium 3: High

REFERENCE BOOKS:	
1.	Gina Wisker, "The Undergraduate Research Hand book", 2018.
E Resource	
1.	https://www.coursera.org/learn/academic-writing-capstone

ANALOG VLSI DESIGN LAB

Course Code:	**22VDE204**	**Course Type:**	**PCC Lab**
Teaching Hours/Week (L: T: P)	**0:0:2**	**Credits:**	**01**
Total Teaching Hours:	**0+0+26**	**CIE + SEE Marks:**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To design amplifier for the given specifications.
2.	Perform schematic and layout simulations using available tool.

List of Experiments

Tool to be used: CADENCE/SYNOPSYS/MENTOR GRAPHICS

1.	Design a single stage amplifier using MOSFETs for the given specifications.
2.	Design a differential amplifier using MOSFETs for the given specifications.
3.	Design a two-stage op-amp for the given specification. Determine the frequency response, CMRR, gain margin, phase margin, UGBW and slew rate.
4.	Mini project using the above circuits as sub blocks.

Course Outcomes: At the end of the course student will be able to

1.	Design single stage amplifier and op-amp for the given specifications.
2.	Design and implement analog block.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE204.1	2	2	2	-	3	-	2	-
22VDE204.2	2	2	2	-	3	-	2	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, TMH, 2007
2.	R. Jacob Baker, Harry W. Li., David E. Boyce, “CMOS: Circuit Design, Layout and Simulation”, PHI, 2003.

E Resources

1.	http://www-classes.usc.edu/engr/ee-s/477p/cadencetutorial.pdf
2.	https://www.academia.edu/5272241/The_ECE_218_Analog_VLSI_Circuit_Design_CMOS_Operational_Amplifier

REAL TIME OPERATING SYSTEMS LAB

Course Code:	**22VDE205**	**Course Type:**	**PCC Lab**
Teaching Hours/Week (L: T: P):	**0:0:2**	**Credits:**	**01**
Total Teaching Hours:	**0+0+26**	**CIE + SEE Marks:**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	Learn the RTOS programming in RT-Linux
2.	Implement mini project in RTOS concepts.

List of Experiments

1.	Write a program for Thread Creation and Termination.
2.	Create independent threads each of which will execute some function and wait till threads are complete before main continues. Unless we wait run the risk of executing an exit which will terminate the process and all threads before the threads have completed.
3.	Create the N number of threads and find the how many threads are executed.
4.	Create threads numbers 1-3 and 8-10 as permitted by functionCount1 and create threads number 4-7 as permitted by functionCount2 and print final count value.
5.	Design and execute a program using any thread library to create the number of threads specified by the user, each thread independently generates a random integer as an upper limit and then computes and prints the number of primes less than or equal to that upper limit, along with that upper limit.
6.	Rewrite Program 5, such that the processes instead of thread are created and the number of child processes created is fixed as two. The program should make use of kernel timer to measure and print the real time, processor time, User space time and kernel space time for each process.
7.	Design, develop and implement a process with a producer thread and a consumer thread which make use of a bounded buffer (Size can be prefixed at suitable value) for communication. Use any suitable synchronization construct.
8.	Design, develop and execute a program to solve a system of n liner equations using successive over-relaxation method and n processes which use shared memory API.

Course Outcomes: At the end of the course student will be able to

1.	Understand the RTOS programming in RT-Linux
2.	Develop RTOS mini projects from the concepts learned.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / ↓ Course Outcomes	1	2	3	4	5	6	PSO↓ 1	PSO↓ 2
22VDE205.1	1	2	3	-	-	3	-	3
22VDE205.2	3	2	3	-	-	3	-	3

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Sam Siewert, John Pratt, "Real-Time Embedded Components and Systems with Linux and RTOS", Mercury Learning and Information, 2015.
2.	Raj Kamal, "Embedded System- Architecture, programming and Design", 2nd Edition, Tata McGraw-Hill Education Pvt. Ltd., 2008.
3.	Dreamtech Software Team, "Programming for Embedded Systems", John Wiley, India Pvt. Ltd., 2008.

E Resources

1.	http://cs.uccs.edu/~cchow/pub/rtl/doc/html/GettingStarted/
2.	https://www.coursera.org/learn/real-time-systems#syllabus
3.	https://www.udemy.com/course/real-time-operating-system/
4.	https://tldp.org/HOWTO/RTLinux-HOWTO.html#toc4

DESIGN FOR IOT AND CLOUD COMPUTING

Course Code:	**22VDE211**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**2:0:2**	**Credits**	**03**
Total Teaching Hours	**26+0+26**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	Understand the basic concepts of IoT and its architecture.
2.	Understand the cloud and fog computing in IoT.
3.	Understand the design of IoT system.

UNIT-I

11 Hours

Introduction to the Internet of Things: Internet of Things Concepts, IoT Framework, Information and Communication Technology Infrastructure, Standards.

Enabling Technologies for the Internet of Things: IP Based IoT, Physical/ Link Layer, Network Layer, Transport Layer, Application layer.

UNIT-II

10 Hours

Interoperability and Discoverability: The Verticals: Cloud-Based Solutions, HTTP Protocol, UPnP Protocol, Messaging Queues and Publish/ Subscribe Communications, CoAP Protocol Service and Resource Discovery.

Cloud and Fog Computing in the Internet of Things: IoT System Requirements, Cloud Computing in IoT, Big Data Processing Pattern, Big Stream, Big Stream and Security, Fog Computing in IoT, The Role of IoT Hub.

UNIT-III

05 Hours

A Tutorial Introduction to IoT Design and Prototyping with Examples: Hardware for IoT, Main Features of IoT Hardware Development Platforms, Software for IoT, Design and Prototyping of IoT Applications, Projects on IoT Applications.

List of Experiments

1. Developing a local web server on IoT Platform
2. Device control using IoT platform using local webserver on a HTML web page
3. Illustration of CoAP protocol
4. Illustration of HTTP protocol on a IoT application
5. Demonstration of MQTT protocol in IoT application

6. Application of IEEE. 802.11, IEEE 802.5 communication in IoT platform

Course Outcomes: At the end of the course student will be able to

1.	Explain IoT; Describe the IoT framework, Information and Communication Technology Infrastructure and Standards.
2.	Describe IP based IoT and explain the enabling technologies of IoT.
3.	Explain the interoperability and discoverability of IoT systems.
4.	Describe the Cloud and Fog computing techniques in IoT.
5.	Design and develop prototype of an IoT system.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE211.1	3	1	-	2	1	-	-	2
22VDE211.2	3	1	-	2	1	-	-	2
22VDE211.3	3	-	-	-	-	-	-	2
22VDE211.4	3	-	-	-	-	-	-	1
22VDE211.5	3	-	-	-	-	-	-	1

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Qusay F. Hassan, “Internet of Things A to Z, Technologies and Applications”, John Wiley Publications, 2018.
2.	Simone Cirani, Gianluigi Ferrari, Marco Picone, Luca Veltri, “Internet of Things, Architectures, Protocols and Standards”, John Wiley Publications, 2019.
3.	Donald Norris, “Internet of Things: Do-it-Yourself Projects with Arduino, Raspberry Pi, and BeagleBone Black”, McGraw-Hill Education Publications, 2015.

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/106/105/106105166/
2.	https://nptel.ac.in/courses/108/108/108108098/

MEMS AND IC INTEGRATION

Course Code:	**22VDE212**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To give an overview of MEMS and its application
2.	To give an overview of CMOS compatible MEMS Fabrication techniques
3.	To explain the scaling effects in Microsystems
4.	To introduce the different signal conditioning circuits for MEMS
5.	To perform the case study of several MEMS Devices

UNIT-I

Introduction to MEMS and MEMS fabrication	**15 Hours**

Introduction: Micro Sensors, Actuators, Systems and Smart Materials: An Overview

Application of MEMS -Silicon Capacitive Accelerometer, Piezoresistive Pressure Sensor, Conductometric Gas Sensor, Fiber-Optic Sensors, Microsystems at Radio Frequencies.

CMOS Compatible MEMS Fabrication- Lithography, Etching, Silicon Micromachining.

UNIT-II

Scaling Effects in Microsystems	**15 Hours**

Scaling in the Mechanical Domain, Scaling in the Electrostatic Domain, Scaling in the Magnetic Domain, Scaling in the Thermal Domain, Scaling in Design and Simulation. MEMS system-level design methodology, Techniques for sensing and actuation, Electronics Circuits for Micro and Smart Systems- Signal Conditioning circuits, Practical Signal conditioning Circuits for Microsystems.

UNIT-III

Case Study of MEMS Devices	**10 Hours**

Pressure Sensors, Inertial Sensors, Piezoelectric Transducers, RF MEMS, Accelerometer with transducer.

Course Outcomes: At the end of the course student will be able to

1.	Explain the MEMS devices and its application.
2.	Discuss the CMOS compatible MEMS Fabrication techniques.
3.	Explain the scaling effects in Microsystems.

4.	Discuss the different signal conditioning circuits for MEMS.
5.	Perform the case study of several MEMS Devices.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE212.1	-	-	2	3	2	-	2	-
22VDE212.2	-	-	2	3	2	-	2	-
22VDE212.3	-	-	2	3	2	-	2	-
22VDE 212.4	-	-	2	3	2	-	2	-
22VDE212.5		-	2	3	2	-	2	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	G.K. Ananthasuresh, K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K.Aatre "Micro and Smart Systems Technology and Modeling", John Wiley and Sons 2009.
2.	Stephen D. Senturia, "Microsystem Design", Kluar Publishers, 2001.
3.	Nadim Maluf, "An Introduction to Microelectromechanical Systems Engineering", Artech House, 2000.

E Books / MOOCs/ NPTEL

1.	https://onlinecourses.nptel.ac.in/noc19_ee40

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Course Code:	**22VDE213**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	Understand graph optimization problems, logic minimization using Boolean algebra.
2.	Know HDLs synthesis optimization techniques, architectural level synthesis and optimization techniques.
3.	Know logic minimization algorithms and techniques, optimization principles for two level and multi-level combinational logic.
4.	Know to evaluate delay in logic networks and apply delay minimization algorithms.
5.	Understand sequential circuit optimization and algorithms for area optimal library binding.

UNIT-I

Graphs	**15 Hours**

Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

HDLs used in synthesis, abstract models, logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Architectural synthesis: circuit specifications, strategies for architectural optimization, scheduling with timing constraints and resource constraints.

UNIT-II

Optimization	**15 Hours**

Two level combinational logic optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization, Boolean relations.

Multiple level combinational optimizations: Models and transformations for combinational networks, algebraic model

Algorithm for delay evaluation and optimization, rule based system for logic optimization.

UNIT-III

	10 Hours

Sequential circuit optimization: Sequential circuit optimization using state-based models, sequential circuit optimization using network models.

Cell library binding: algorithms for library binding, covering algorithms based on structural matching, rule-based library binding.

Course Outcomes: At the end of the course student will be able to

1.	Analyze and optimize graph optimization problems, logic minimization using Boolean algebra.
2.	Understand HDLs synthesis optimization techniques, architectural level synthesis and optimization techniques.
3.	Explain and apply logic minimization algorithms and techniques, optimization principles for two level and multi-level combinational logic.
4.	Evaluate delay in logic networks and apply delay minimization algorithms.
5.	Apply state-based model and network-based model for sequential circuit optimization, algorithms for area optimal library binding.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE213.1	2	-	2	2	3	-	3	-
22VDE213.2	2	-	2	2	3	-	3	-
22VDE213.3	2	-	2	2	3	-	3	-
22VDE213.4	2	-	2	2	3	-	3	-
22VDE213.5	2	-	2	2	3	-	3	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Giovanni De Micheli, “Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.
2.	Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, “Logic Synthesis”, McGraw-Hill, USA, 1994.

DSP ALGORITHMS AND ARCHITECTURE

Course Code:	**22VDE221**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To understand the concepts of digital signal processor functional units.
2.	To understand the filter structures implementation on DSP processors.
3.	To perform array processing using the array processing architectures.
4.	To understand the audio coding algorithms and standards.

UNIT-I

Basic Architectural Features	**15 Hours**

Performance and Structural limitations. Measures and Structures for enhancing performance. Introduction to VLIW architecture

Survey of DSP processors of Intel, Texas Instruments and Motorola.

UNIT II

Instruction set of TMS54xx processors	**15 Hours**

Filter structures, Transform structures, Data Flow and Control flow issues, Array processing approaches to DSP solutions.

UNIT-III

Implementation of various DSP algorithms Applications	**10 Hours**

Introduction to audio coding, MPEG audio coding, MPEG advanced audio coding, Dolby AC3.

Course Outcomes: At the end of the course student will be able to

1.	Choose DSP core for generic DSP applications.
2.	Develop filter structures and transform structures for the given DSP system.
3.	Apply array processing approaches to DSP solutions.
4.	Develop filter structures and transform structures for signal processing applications.
5.	Understand the audio coding standards and algorithms.

Course Outcomes Mapping with Program Outcomes & PSO

	Program Outcomes→	1	2	3	4	5	6	**PSO↓**	

↓ Course Outcomes							1	2
22VDE221.1	3	-	3	-	-	-	-	2
22VDE221.2	3	-	3	-	-	-	-	2
22VDE221.3	3	-	3	-	-	-	-	2
22VDE221.4	3	-	3	-	-	-	-	2
22VDE221.5	3	-	3	-	-	-	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Peter Pirsch, “Architectures for Digital Signal Processing”, Wiley, 2004.
2.	Khalid Sayood, “Introduction to Data Compression”, Morgan Kaufman
3.	Ifeachor E. C., Jervis B. W, “Digital Signal Processing: A practical approach”, Pearson-Education, PHI/ 2002.
4.	B Venkataramani and M Bhaskar, “Digital Signal Processors”, TMH, 2nd, 2010.

EMBEDDED CONTROLLER PROGRAMMING FOR REAL-TIME SYSTEMS

Course Code:	**22VDE222**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To develop an understanding of various Real Time systems
2.	To give the students a thorough exposure to ARM processors and the PIC18 microcontrollers
3.	To program PIC microcontroller for different applications and also to Interface sensors, transducers, motors, relays, and various input/output devices with PIC microcontrollers

UNIT-I

Introduction to real-time systems	**14 Hours**

Introduction, Real-time systems development, Microprocessors and real-time applications, Definition of a real-time system, Functional Requirements, Temporal Requirements, Classification of Real-Time Systems, The Real-Time Systems Market.

UNIT-II

ARM Processors	**08 Hours**

Introduction, History of ARM Processors, Basic Architecture and organization of Cortex-M3 processor, ARM Processor (Cortex-M3) Fundamentals: Registers, Application Program. Status Register: Current Program Status Register, Pipeline (3-stage pipeline ARM organization, 5-stage pipeline ARM organization).

The PIC18 Microcontrollers	**08 Hours**

History and Features, PIC18 Architecture, Assembly Language Programming: Branch, Call and Time Delay Loop PIC18 I/O Port Programming Arithmetic, Logic Instructions and Programs, Bank Switching, Table Processing, Macros, and Modules, PIC18 Programming in C, PIC18 Hardware Connections and ROM Loaders.

UNIT-III

PIC18 Interfacing	**10 Hours**

PIC18 Timer Programming in Assembly and C, Serial Port Programming in Assembly and C Interrupt Programming in Assembly and C, LCD and Keyboard Interfacing, ADC, DAC, and Sensor Interfacing, SPI Protocol and DS1306 RTC Interfacing, Motor Control: Relay, PWM, DC, and Stepper Motors.

Course Outcomes: At the end of the course student will be able to

1.	Develop an understanding of various Real Time systems Application

2.	Obtain a broad understanding of the technologies and applications for the emerging and exciting domain of real-time systems
3.	Understand and analyze the features of ARM processors and Applications.
4.	Understand and analyze the features of PIC18 microcontrollers and Applications.
5.	Interface I/O devices with PIC18 microcontroller.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE222.1	1	1	1	-	-	3	-	2
22VDE222.2	1	1	1	-	-	3	-	2
22VDE222.3	1	1	1	-	-	3	-	2
22VDE222.4	1	1	2	-	-	3	-	2
22VDE222.5	1	1	2	-	-	3	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Hermann Kopetz, "Real-Time Systems, Design Principles for Distributed Embedded Applications", 2nd Edition, Springer New York, NY.
2.	Jane W. S. Liu, "Real-Time Systems", PHI (13 April 2000).
3.	John B. Peatman, "Design with PIC Micro controller", Pearson Education, 1988.
4.	Steave Furber, "ARM system - on - chip architecture", Addison Wesley, 2000.
5.	Jonathan W Valvano, "Embedded Systems: Introduction to ARM Cortex™-M3 Microcontroller", Volume1, CreateSpace Independent Publishing Platform, 2012.
6.	Muhammad Ali Mazidi, Rolin D. McKinlay, "PIC Microcontroller", Danny Causey Pearson Education.

E Books / MOOCs/ NPTEL

1.	https://nptel.ac.in/courses/108105057
2.	https://nptel.ac.in/courses/108102045

SYSTEM VERILOG FOR VERIFICATION AND TESTING

Course Code:	**22VDE223**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To understand system Verilog language features and its applications
2.	To learn about Universal Verification Methodology Concepts
3.	To learn how to verify Design-Under Test (DUT) using SV and UVM
4.	To gain hands-on understanding about system Verilog and UVM
5.	To develop testbenches in system Verilog independently

UNIT-I

Introduction to System Verilog	**15 Hours**

Language basics: Verification Guidelines, Data Types, Arrays, Ques, Structures, Union, Packages, Class, Module, Program, Interface, Operators.

Advance features: Constrained Random Test Generation and Verification, Assertions, Functional Coverage, Process, Procedural Programming Statements, Inter-Process Synchronization, Semaphores and Mailboxes, Clocking Blocks, Checkers, Tasks and Functions.

UNIT-II

Introduction to UVM	**15 Hours**

UVM Basics: The Structure of UVM testbenches and components, UVM Library Basics, the basic concepts and components that make up a standard reusable interface environment.

UVC development and Usage, The creation of simple testbenches, Various techniques for sequence and randomization control.

Advanced Concepts: A methodology and automation to enable productive and reusable register related verification logic. How to wrap device specific logic and reuse it in block, sub-system and system integration.

UNIT-III

SV/UVM Verification Practice Examples	**10 Hours**

Testbench Connection Examples, Messaging Example, Sequence Example, Analysis Example, Register Example, Functional Coverage Example, Testbench Build Example, Slave agent Example.

Course Outcomes: At the end of the course student will be able to

1.	Understand system Verilog applications

2.	Understand the concept of UVM
3.	Verify DUT using SV and UVM
4.	Understand system Verilog and UVM
5.	Develop testbenches independently

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE223.1	3	1	1	-	1	-	2	-
22VDE223.2	3	1	1	-	1	-	2	-
22VDE223.3	3	1	1	-	1	-	2	-
22VDE223.4	3	1	1	-	1	-	2	-
22VDE223.5	3	1	1	-	1	-	2	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Ashok B. Mehta, "Introduction to System Verilog", Springer – 2021
2.	Sharon Rosenberg, Kathleen Meade, "A practical guide to adopting Universal Verification Methodology", Cadence Design Systems – USA.
3.	UVM CookBook - by Siemens
4.	Chris Spear, "System Verilog for Verification", 2nd Edition, Springer.

DIGITAL CONTROL IN SWITCHED MODE POWER CONVERTERS & FPGA-BASED PROTOTYPING

Course Code:	**22VDE231**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**1:0:4**	**Credits**	**03**
Total Teaching Hours	**15+0+52**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics & Communication Engineering

Course Objectives:

1.	To know about latest digital control trends in power electronics industries.
2.	To understand benefits of digital control, modulation, and digital control architectures.
3.	To understand embedded control implementation platforms.
4.	To understand Verilog HDL and fixed-point implementation,
5.	To understand hardware development and FPGA-based prototyping.

Prerequisites:

UNIT-I

Introduction to digital control in switched mode power converters (SMPCs), Fixed and variable frequency digital control architectures, MATLAB custom model development for simulation under digital control, Modelling techniques and model validation using MATLAB, Frequency and time domain digital control design approaches	**16 Hours**

UNIT-II

Digital control implementation blocks and steps for FPGA based prototyping, Introduction to Verilog HDL and simulation using Xilinx, Webpack Digital controller implementation using fixed point arithmetic and Verilog HDL, Digital Control Implementation using STM32 and C2000 Series Microcontrollers, Steps for FPGA prototyping of digital voltage mode and current mode control	**16 Hours**

UNIT-III

Design and validation case studies using digital voltage and current mode control, Hardware case studies of advanced digital control techniques	**08 Hours**

Course Outcomes: At the end of the course student will be able to

1.	Design and Implement FPGA/Microcontroller-based Digital Control for Switched Mode Power Converters.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDE231.1	3	1	2	2	2	2	3	3

1: Low 2: Medium 3: High

SEE is LAB based if offered in the institution.

REFERENCE BOOKS:

1.	S. Kapat and P. T. Krein, "A Tutorial and Review Discussion of Modulation, Control and Tuning of High Performance DC-DC Converters based on Small-Signal and Large-Signal Approaches", IEEE Open Journal of Power Electronics, vol. 1, pp. 339 - 371, Aug. 2020.
2.	R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics", 3rd Ed., Springer, 2020.

E Books / MOOCs/ NPTEL

1.	https://onlinecourses.nptel.ac.in/noc22_ee124/
2.	STM32 Reference Manual
3.	C2000 Design Resources

DISTRIBUTED COMPUTING

Course Code:	**22VDE232**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	Explain the various distributed systems and its architectures
2.	Discuss various process and communication aspects in the distributed systems
3.	Discuss naming conventions and analyse various clock synchronization
4.	Describe the consistency and replication, fault tolerance and security aspects
5.	Illustrate the use of Distributed-Object based Systems, Distributed File Systems and Distributed Web-based Systems in real world applications

UNIT-I

Introduction and Architecture	**14 Hours**

Introduction: Introduction to distributed systems, goals, types of distributed systems

Architecture: Architectural styles, system architectures, architectures versus middleware, self-management in distributed systems

Processes: Threads, virtualization, clients, servers, code migration

Communication: Remote procedure calls, message-oriented communication, stream-oriented communication, multicast communication

UNIT-II

Design of Distributed Systems	**16 Hours**

Naming: Names, identifiers and addresses; flat naming, structured naming, attribute-based naming

Synchronization: Clock synchronization, logical clocks, mutual exclusion, global positioning of nodes, election algorithms

Consistency and Replication: Introduction; data-centric consistency models; client-centric consistency models; replica management; consistency protocols

Fault Tolerance: Introduction; process resilience; reliable client-server communication; reliable-group communication; distributed commit; recovery

Security: Introduction; secure channels; access control; security management

UNIT-III

Distributed system Models	**10 Hours**

Distributed-Object based Systems: Architecture; Processes; Communication; Naming; Synchronization; Consistency and Replication; Fault Tolerance; Security

Distributed File Systems: Architecture; Processes; Communication; Naming; Synchronization; Consistency and Replication; Fault Tolerance; Security

Distributed Web-based Systems: Architecture; Processes; Communication; Naming; Synchronization; Consistency and Replication; Fault Tolerance; Security

Course Outcomes: At the end of the course student will be able to

1.	Apply the concepts of distributed computing systems considering different architectural styles.
2.	Analyze the various process and communication aspects in the distributed systems.
3.	Apply naming conventions and analyze various clock synchronization needed for distributed systems.
4.	Design applications for consistency and replication, fault tolerance and security aspects.
5.	Make use of Distributed-Object based Systems, Distributed File Systems and Distributed Web-based Systems in real world applications.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2		4	5	6	**PSO↓** 1	2
22VDE232.1	-	-	2	-	-	1	-	1
22VDE232.2	-	-	2	-	-	1	-	2
22VDE232.3	-	-	2	-	-	1	-	1
22VDE232.4	1	-	2	-	-	1	-	1
22VDE232.5	1	-	2	-	-	1	-	2

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Andrew S. Tanenbaum, Maarten Van Steen, "Distributed Systems: Principles and Paradigms", Pearson, 2007.
2.	George Coulouris, Jean Dollimore and Tim Kindberg, "Distributed Systems: Concepts and design", Pearson, 2011.
3.	Pradeep K. and Sinha, "Distributed Operating System: Concepts and Design", PHI, 2009.
4.	Andrew S. Tanenbaum, "Distributed Operating System", Pearson, 2008.

E Books / MOOCs/ NPTEL

1.	https://archive.nptel.ac.in/courses/106/106/106106168/
2.	https://archive.nptel.ac.in/courses/106/106/106106107/

Scripting Languages for VLSI

Course Code:	**22VDE233**	**Course Type**	**PEC**
Teaching Hours/Week (L: T: P)	**3:0:0**	**Credits**	**03**
Total Teaching Hours	**40+0+0**	**CIE + SEE Marks**	**50+50**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	To understand the concepts of scripting languages for developing web-based projects.
2.	To Illustrates object-oriented concepts like TCL, PERL.
3.	To understand security issues.
4.	To learn the concept of verification.

UNIT-I

Automatic code generation	**05 Hours**

Report Filtering, Netlist patching, Test Vector Generation. Controlling

Tools.

PEARL	**10 Hours**

History and concepts of PERL, Scalar Data, Arrays and List Data, Control structures, Hashes, Basics I/O, Regular Expressions, Functions.

UNIT-II

Tool Command Language	**10 Hours**

TCL Structure, syntax, Variables and Data in TCL, Control Flow, Procedures, strings, patterns.

TK	**05 Hours**

TK Fundamentals: Hello World in Tk, Naming Tk Widgets, Configuring Tk Widgets, About The Tk Man Pages, Summary Of The Tk Commands.

UNIT-III

Verification	**10 Hours**

Introduction to verification, Verification Process Specification, Design Decomposition, Functional Test Strategies, Transformation Test Strategies, Coverage.

Course Outcomes: At the end of the course student will be able to

1.	Understand the differences between scripting languages.
2.	Understand the general features of PERL scripting language.
3.	Explain syntax and variables in TCL.

4.	Identify the TK widgets and commands.
5.	Get familiarized with verification methodology of VLSI circuits.

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→ / **↓ Course Outcomes**	1	2	3	4	5	6	**PSO↓** 1	2
22VDE233.1	1	2	1	-	-	-	2	-
22VDE233.2	2	3	1	1	-	-	2	-
22VDE233.3	2	1	1	1	-	-	2	-
22VDE233.4	2	1	1	-	-	-	-	-
22VDE233.5	2	3	1	-	2	-	2	-

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Wall, L. and Schwartz, R., "Programming perl", Sebastopol: O'Reilly, 2000.
2.	The World of Scripting Languages, David Barron, Wiley Publications.
3.	B.B. Welch, K. Jones, J. Hobbs, "Practical programming in TCL and Tk", Prentice Hall PTR, Upper Saddle River, N.J, 2014.
4.	Bening, L., "Principles of verifiable rtl design", Springer, 2001.
5.	Ousterhout, J. and Jones, K., "TCL and the Tk toolkit", Upper Saddle River, NJ: Addison-Wesley, 2011.

LABVIEW

Course Code:	**22VDEAU21**	**Course Type:**	**AUDIT**
Teaching Hours/Week (L: T: P)	**1:0:1**	**Credits:**	**-**
Total Teaching Hours:	**13+0+26**	**CIE + SEE Marks:**	**-**

Teaching Department: Electronics and Communication Engineering

Course Objectives:

1.	Understanding LabVIEW terminologies and dataflow in LabVIEW.
2.	Building VIs to collect analyze IO data in LabVIEW.

List of Experiments

1.	**Navigating LabVIEW:** Introduction to LabVIEW, Project explorer, Parts of VI, Front panel, Block diagram, Controls, VIs, Functions, Dataflow in LabVIEW.
2.	**Debugging VIs:** Correcting broken VIs, Organizing VIs, Debugging Techniques, Undefined or unexpected data, Error Handling.
3.	**Building basic VI:** Front panel basics, LabVIEW Data types, while loops, For loops, Timing in VI, Data Feedback in loops, Plotting data- waveforms and charts, Case Structures, Event driven programming.
4.	**Developing Modular Applications:** Understanding modularity, building icons and Connector pane, using Sub VIs.
5.	**Creating and Leveraging Data structures:** Arrays, Common Array functions, Polymorphism, Auto-indexing in arrays, Clusters and Type definitions.
6.	**Managing File and Hardware Resources:** Understanding Hardware and Software resources, File I/O functions, Measuring fundamentals with DAQ.
7.	**Using sequential and state Machine Algorithms:** Using sequential and state programming, State machines.
8.	**Solving Dataflow Challenges with Variables:** Communication between parallel loops, writing controls and reading from indicators, Variables, Race conditions.
9.	**Navigating LabVIEW:** Introduction to LabVIEW, Project explorer, Parts of VI, Front panel, Block diagram, Controls, VIs, Functions, Dataflow in LabVIEW.
10.	**Debugging VIs:** Correcting broken VIs, Organizing VIs, Debugging Techniques, Undefined or unexpected data, Error Handling.
11.	**Building basic VI:** Front panel basics, LabVIEW Data types, While loops, For loops, Timing in VI, Data Feedback in loops, Plotting data- waveforms and charts, Case Structures, Event driven programming.

12.	**Developing Modular Applications:** Understanding modularity, Building icons and Connector pane, using Sub VIs.

Course Outcomes: At the end of the course student will be able to

Course Outcomes Mapping with Program Outcomes & PSO

Program Outcomes→	1	2	3	4	5	6	**PSO↓**	
↓ Course Outcomes							1	2
22VDEAU21.1	-	2	1	-	-	1	-	1
22VDEAU21.2	2	2	3	-	-	1	-	1

1: Low 2: Medium 3: High

REFERENCE BOOKS:

1.	Jovitha Jerome, "Virtual Instrumentation using LabVIEW", PHI Learning Private Limited, 2010.
2.	Robert H. Bishop, "Learning with LabVIEW", Pearson, 2015.

E Resources

1.	https://www.ni.com/getting-started/labview-basics/
2.	https://www.labviewmakerhub.com/doku.php?id=learn:tutorials:labview:basics
3.	http://ece-research.unm.edu/jimp/415/labview/LV_Intro_Six_Hours.pdf