SYLLABUS FOR M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (AUTONOMOUS) [2015 Scheme]

NMAM INSTITUTE OF TECHNOLOGY
(An Autonomous Institution under VTU, Belgaum)

Syllabus of
Master of Technology
in
VLSI DESIGN & EMBEDDED SYSTEMS
Effective 2015-2016

Department of
Electronics and Communication Engineering
## SCHEME OF TEACHING AND EXAMINATION FOR VLSI AND EMBEDDED SYSTEM DESIGN - 2015 SCHEME

### I SEMESTER

<table>
<thead>
<tr>
<th>Sub. code</th>
<th>Name of the Subject</th>
<th>L+T+P+S</th>
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<th>Contact Hrs/Week</th>
<th>Duration of Sem End Exam in hours</th>
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### ELECTIVE – I

- 15VDE111 Modeling of Digital Systems using VHDL
- 15VDE112 High Speeds VLSI Design
- 15VDE113 SoC Design

### ELECTIVE – II

- 15VDE121 Advanced Digital System Design
- 15VDE122 DSP Algorithms & Architecture
- 15VDE123 Soft Computing
## II SEMESTER

<table>
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### ELECTIVE – III

- 15VDE211 Advanced Microcontroller
- 15VDE212 Algorithms for VLSI
- 15VDE213 Low Power VLSI

### ELECTIVE – IV

- 15VDE221 System Design Using Embedded Processors
- 15VDE222 MEMS and IC Integration
- 15VDE223 VLSI Signal Processing
### III SEMESTER

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<td>Full time 8 weeks</td>
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<td>15VDE302</td>
<td>Seminar</td>
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<td>15VDE303</td>
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<td>Project -part II</td>
<td>14 weeks</td>
<td>Report 100</td>
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**GRAND TOTAL from 1st to 4th semester: 100 credits**

**NOTE:**

1. 15VDE301: Industrial Training/mini-project: Practical training report and oral presentation are to be evaluated by the Department for 50 marks each. Alternatively, if mini-project is carried out, it is evaluated for 100 marks by the Department.

2. 15VDE302: The Seminar Marks are to be awarded by the Department committee constituted for the purpose.
3. 15VDE303: Progress of work to be assessed by the Department Committee including the guide for 100 marks.

4. 15VDE401: The project report valuation will be carried out separately by the guide for 50 marks, Department Committee for 50 marks (total IA marks 100) and the external examiner for 100 marks. Viva-Voce will carry 200 marks and will be conducted by a committee consisting of the following:
   a. Chairman, BOE (PG) or his nominee,
   b. Project Guide and External examiner
I - SEMESTER

ADVANCED EMBEDDED SYSTEMS

<table>
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Course Outcomes:

At the end of the course the student should be able to:

1. Understand General structure of an Embedded System.
2. Realize the characteristics of an Embedded System.
3. Identify Problems and Design challenges in Embedded System.
4. Lear IDE and Program using embedded C.
5. Understand the overview of RTOS.

UNIT-I


8 Hrs

UNIT-II


10 Hrs

UNIT-III

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Programming in Embedded C

12 Hrs

UNIT-IV

Real-Time Operating System (RTOS) based Embedded System Design:

Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS (Self Study/Case Study).

12 Hrs
UNIT-V

The Embedded System Development Environment: The Integrated Development Environment (IDE) (Self Study/Case Study), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Trends in the Embedded Industry: (Self Study/Case Study), Processor Trends in Embedded Systems, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks. 10 Hrs

Reference Books:

CMOS VLSI DESIGN

Subject Code  15VDE102
Credits  5
Hours/Week  4+0+2+0
CIE  50 Marks
Total Hours  52
SEE  50 Marks

Course Outcomes:

At the end of the course the student should be able to:

1. Understand the basic details of MOS transistors in terms of its structure, I-V characteristics and design equations.
2. Understand the second order effects in MOS devices such as body effect, channel length modulation, drain punch-through etc.
3. Explain the need for scaling, different types of scaling models and effects of scaling on device parameters. Understand the salient steps in the fabrication of CMOS devices.
4. Design CMOS circuit for latches and flip-flops.
5. Design of sequential circuits with enhancement type and depletion type NMOS load.
6. Design dynamic CMOS and Domino CMOS logic circuits.
7. Understand the phenomenon of CMOS latchup, charge sharing in dynamic CMOS circuits.
8. Develop and perform Verilog simulation of given digital system and schematic simulation of given logic expression.

UNIT-I
MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. Mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, $\beta_n / \beta_p$ ratio, noise margin, static load MOS inverters, differential inverter, tristate inverter, BiCMOS inverter.

UNIT-II
CMOS Process Technology: Semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD, refractory gate, multilayer inter connect), Circuit elements, resistor, capacitor, interconnects, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

UNIT-III

10 Hrs

UNIT-IV

Dynamic Logic Circuits – Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuits techniques, Dynamic CMOS circuit techniques Sheet resistance & standard unit capacitance concepts, delay unit time, inverter delays, driving capacitive loads, propagate delays.

12 Hrs

UNIT-V

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS., Domino CMOS structure and design, Charge sharing, Clocking - clock generation, clock distribution, clocked storage elements.

10 Hrs

Reference Books:

CMOS VLSI DESIGN LAB

(Use any of the EDA Tools)

LAB EXPERIMENTS:

1. Develop Verilog code for the following. Perform simulations using test benches.
   - Universal Gates
   - A transmission gate
   - 4 bit parallel adder
   - MOD-N synchronous counter
   - Asynchronous counter

2. Perform schematic simulation for a CMOS Inverter. Report the result of DC and AC analysis.

3. Perform schematic simulation for a static CMOS circuit to compute $f = \overline{(A+B)(C+D)}$

4. Perform layout simulation for a CMOS inverter.

5. Using SPICE, perform simulation to measure the power for a digital circuit.
VLSI DESIGN VERIFICATION

Subject Code  15VDE103  CIE  50 Marks
Hours/Week  4+0+0+4  SEE  50 Marks
Total Hours  52  Credits  5

Course Outcomes:

At the end of the course the student should be able to:

1. Introduce the concepts and techniques of design verification
2. Understand the technology challenges and verification technology options.
3. Study different approaches for verification methodologies.
4. Understand the concept of manufacturing tests of digital circuits.
5. Understand fault modeling, simulation, Automatic Test Pattern Generation, BIST etc

UNIT-I
Introduction: VLSI development process, role of testing and verification, verification methodology, Types of Design Verification - Functional Verification, Simulation Emulation.

UNIT-II
Block-level Verification. Functional Verification through simulation. Whitebox, blackbox and Graybox testing. Verilog/VHDL test bench for functional verification. 12 Hrs

UNIT-III
Static Timing Verification. Concept of static timing analysis. Timing constraints, timing models, critical path analysis, false paths.
Physical Design Verification. Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, cross talk. 10 Hrs

UNIT-IV
Fault modeling: defects, errors & fault, Functional Versus Structural Testing, fault models, single stuck at faults
Logic and fault simulation: Modeling circuit for simulation, event driven simulation, serial fault simulation 10 Hrs

UNIT-V
Testing and verification: how to test chips? VLSI Technology Trends Affecting Testing, test equipments, electrical parametric testing 10 Hrs

Test generation & DFT: ATPG for combinational circuit, Design for testability and scan, scan cell design, BIST 10 Hrs

Reference Books:

R2. Prakash Rashinkar, Peter Paterson and Leena Singh “System-on-a-Chip Verification – Methodology and
R5. “An Excellent Source for Instructors for Formal Verification Techniques” (website developed by) Prof. V. Narayanan, Penn State University, USA. http://www.cse.psu.edu/~vijay/verify/instructors.html

APPLICATION LAB – I

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List of Experiments

ARM LAB

1. Digital I/O, MCU pin direction, and logical functions, written in assembly and simulated
2. LEDs and switching, written in assembly (simulated)
3. Use switches and LEDs, and control LED intensity using switches written in C (simulated)
4. Traffic Light Controller with bits, written in assembly (simulated)
5. Program simple loops and subroutines in C (simulated)
6. Reset system using watchdog timer in case of error.
7. Fixed point arithmetic in assembly
8. Simple FSM simulator in C
ELECTIVE-I

MODELING OF DIGITAL SYSTEMS USING VHDL

Subject Code  15VDE111
Hours/Week  4+0+0+2
Total Hours  52

CIE  50 Marks
SEE  50 Marks
Credits  4

Course Outcomes:

At the end of the course the student should be able to:

Get an insight to the fundamentals of digital logic using Very High Speed Integrated Circuit Hardware Descriptive Language (VHDL).

1. Work on various programs starting with design of basic gates to design of sequential as well as combinational logic circuits using VHDL.
2. Design networks involving arithmetic operations using VHDL language.
3. Analyze and design standard combinational modules.
4. Get an insight to the specification, organization and Implementation of RTL systems.
5. Understand data and control subsystems and able to design it.
6. Analyze the specifications and implement a microcomputer system.
7. Learn to design a RTL system for the specifications mentioned.

UNIT-I

INSIDE VHDL: Introduction to VHDL, Specification of combinational systems using VHDL, Basic language element of VHDL, VHDL description of gates, Behavioral Modeling, Data flow modeling, Structural modeling, Subprograms.  10 Hrs

UNIT-II

DESIGN OF NETWORKS FOR ARITHMETIC OPERATIONS: Design of a Serial Adder with Accumulator, State Graph for Control Network, Design of a Binary Multiplier, Multiplication of a Signed Binary Number, and Design of a Binary Divider with VHDL Codes.  08 Hrs

UNIT-III

STANDARD COMBINATIONAL MODULES: binary decoder, binary encoder, multiplexers and demultiplexers.
UNIT-IV


10 Hrs

UNIT-V

SPECIFICATION AND IMPLEMENTATION OF A MICROCOMPUTER: Basic component of a micro system, memory subsystem, I/O subsystem, Processors, Operation of the computer and cycle time.

12 Hrs

Reference Books:

## HIGH SPEED VLSI DESIGN

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### UNIT-I
Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic  
10 Hrs

### UNIT-II
12 Hrs

### UNIT-III
10 Hrs

### UNIT-IV
Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.  
Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection.  
10 Hrs

### UNIT-V
Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques, Skew Tolerant Design  
10 Hrs

### Reference Books:

# SoC DESIGN

**Sub. Code** 15VDE113  
**CIE Marks** 50

**Hrs./ week** 4+0+0+0  
**SEE Marks** 50

**Total Hrs.** 52  
**Credits** 4

## UNIT-I

12 Hrs

## UNIT-II

**Embedded Processors** - microprocessors, microcontrollers, DSP and their selection criteria. Review of RISC and CISC instruction sets, Von-Neumann and Harward architectures, and interrupt architectures.  
**Embedded Memories** - scratchpad memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.  
10 Hrs

## UNIT-III

**Hardware Accelerators in an SoC** - comparison on hardware accelerators and general-purpose CPU. Accelerators for graphics and image processing.  
**Typical peripherals in an SoC** - DMA controller, USB controller.  
10 Hrs

## UNIT-IV

**Mixed Signal and RF components in an SoC** - Sensors, Amplifiers, Data Converters, Power management circuits, RF transmitter and receiver circuits.  
10 Hrs

## UNIT-V

**SoC Design Flow** - IP design, verification and integration, hardware-software codesign, power management problems, and packaging related problems.  
10 Hrs

## Reference Books:


ELECTIVE-II

ADVANCED DIGITAL SYSTEM DESIGN

Sub. Code 15VDE 121
CIE Marks 50
Hrs./Week 4+0+0+0
SEE Marks 50
Total Hrs. 52
Credits 4

UNIT-I
SEQUENTIAL CIRCUIT DESIGN: Analysis of clocked synchronous sequential circuits and modeling- State diagram, state table, state table assignment and reduction- Design of synchronous sequential circuits-design of iterative circuits- ASM chart and realization using ASM. 12 Hrs

UNIT-II
ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN: Analysis of asynchronous sequential circuit – flow table, reduction-races-state assignment-transition table and problems in transition table- design of asynchronous sequential circuit- Static, dynamic and essential hazards – data synchronizers – mixed operating mode asynchronous circuits – designing vending machine controller. 10 Hrs

UNIT-III

UNIT-IV
SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES: Programming techniques, Reprogrammable device architecture- function blocks, I/O blocks, Interconnects, realize combinational, arithmetic, sequential circuit with PLA, Architecture and application. 10 Hrs

UNIT-V
NEW GENERATION PROGRAMMABLE LOGIC DEVICES: Foldback architecture with GAL, EPLD, EPLA, PEEL; Realization of finite state machine using PLD – FPGA – Xilinx FPGA-Xilinx 4000. 10 Hrs

Reference Books:
DSP ALGORITHMS & ARCHITECTURE

Sub. Code          15VDE122         CIE Marks       50
Hrs./Week           4+0+0+0+0         SEE Marks       50
Total Hrs.          52                Credits              4

UNIT-I

Introduction to Generic DSP's, Performance and Structural limitations. Measures and Structures for enhancing performance.  
12 Hrs

UNIT-II

Filter structures, Transform structures, Data Flow and Control flow issues.  
10 Hrs

UNIT-III

Introduction to Array processing, Array processing approaches to DSP solutions.  
10 Hrs

UNIT-IV

Some modern DSP algorithms (audio, video and multimedia) and development of new computational and arithmetic building blocks.  
10 Hrs

UNIT-V

Architecture development for some Compression and Coding Algorithms. Reference to some standards and development of Architecture based implementation of these.  
10 Hrs

Reference Books:

SOFT COMPUTING

Sub. Code  15VDE123
Hrs./Week  4+0+0+0
Total Hrs.  52

CIE Marks  50
SEE Marks  50
Credits    4

Course Outcomes:

At the end of the course the student should be able to:

1. Answer the situations of real-life such as uncertainty, impression, approximation, partial truth, etc. using nature driven approaches.
2. Develop fuzzy models to solve the wide ranges of uncertainty.
3. Relate and apply global and local optimization methods.
4. Create artificial neural network model in decision support systems.
5. Design computer-aided systems for pattern recognition.

UNIT-I


10 Hrs

UNIT-II


12 Hrs

UNIT-III


10 Hrs

UNIT-IV

NEURAL NETWORKS: Introduction to Neural Network, Adaptive Networks – Feed forward Networks, back propagation algorithm, Self Organizing Maps (SOMs).

10 Hrs
UNIT-V


10 Hrs

Reference Books:

II – SEMESTER

ADVANCES IN VLSI DESIGN

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Course Outcomes:

At the end of the course the student should be able to:

1. Select a suitable semi-custom design approach to design a desired digital system.
2. Analyze the MISFET, MOSFET and MODFETs in equilibrium and under bias.
3. Understand the need for super buffers to drive large capacitive loads.
4. Identify the short channel effects.
5. Design barrel shifter, tally circuit.
6. Apply routing algorithms to determine minimum length path for interconnects.

UNIT- I

Review of MOS Circuits: MOS and CMOS static plots, CMOS switches

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, programmable structure, standard cell approach, Full custom Design, Gate arrays (Self Study/Case Study), Programmable inter connect (Self Study/Case Study) 6 Hrs

MESFET and MODFETs: Structure, operations, quantitative description of MESFETS. 4 Hrs

UNIT-II

MIS Structures and MOSFETs: MIS systems in equilibrium, under bias, small signal operation of MESFETS and small signal analysis of MOSFETS (Self Study/Case Study). 4 Hrs

Super Buffers: NMOS super buffers, NMOS tri-state super buffer and pad drivers, CMOS super buffers, RC delay lines (Self Study/Case Study) 6 Hrs

UNIT-III

Short Channel Effects: Two dimensional Potential profile, High electric field in the short channel, Punch-through and channel length modulation. 6 Hrs

Steering Logic: Driving large capacitive loads, pass-transistor logic, designing pass-transistor logic, Dynamic ratio less inverters, General functional blocks - NMOS and CMOS functional blocks. 5 Hrs
UNIT -IV

Scaling Theory: Constant filed, constant voltage and quasi-constant voltage models

Beyond CMOS: Evolutionary advances beyond CMOS: SOI MOSFET 4 Hrs
Revolutionary advances beyond CMOS: carbon Nano-tubes, Conventional vs. tactile computing, molecular and biological computing.
Molelectronics-Molecular Diode and diode- diode logic 5 Hrs
Defect tolerant computing (Self Study/Case Study).

Challenges to CMOS: Processing Challenges to Further CMOS Miniaturization (Self Study/Case Study).

UNIT-V

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logics, NMOS, CMOS Multiplexers, Barrel shifter. 7 Hrs
Wire routing Algorithms: Need for algorithms, study of Lee-Moore Maze running algorithm and line search algorithm. 5 Hrs

Reference Books:

DESIGN OF ANALOG & MIXED MODE VLSI CIRCUITS

Sub. Code: 15VDE202
Hrs./Week: 4+0+2+0
Total Hrs.: 52
CIE Marks: 50
SEE Marks: 50
Credits: 5

Course Outcomes:

At the end of the course the student should be able to:

1. Design and analyze single stage amplifiers using MOSFETs.
2. Design and analyze differential amplifiers using MOSFETs.
3. Design and analyze operational amplifiers using MOSFETs.
4. Analyze the high frequency behavior of analog small signal amplifier using MOSFETs.
5. Implement oscillators and voltage controlled oscillator (VCO) in CMOS technology.
6. Implement PLL and its applications in CMOS technology.

UNIT-I
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models. MOS Device as a Capacitor

UNIT-II
Single stage Amplifier: CS stage with resistance load, diode connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascode stage, Folded cascode, choice of device models.

UNIT-III
Differential Amplifiers: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell.
Passive and active Current mirrors: Basic current mirrors, Cascade current mirrors, active current mirrors.

UNIT-IV
Frequency response of Amplifier: General considerations, Common source stage, source follower, Common gate stage, Cascode stage and Difference pair. Noise in CS stage, CG stage, source follower, cascode stage, differential pair.

UNIT-V
Operational Amplifiers: One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compensation of two stage OP-Amp, Other compensation techniques.
Oscillators: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO.
PLL: Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications.

Reference Books:

ANALOG & MIXED MODE VLSI LAB

LAB EXPERIMENTS:

TOOLS TO BE USED: CADANCE/SYNOPSIS/MENTOR GRAPHICS.

1. Design a single stage amplifier using MOSFETs for the given specifications.
2. Design a differential amplifier using MOSFETs for the given specifications.
3. Design a two stage op-amp for the given specification. Determine the frequency response, slew rate, offset effects and Noise.
4. Design a simple sample and hold circuit and measure the switching times.

NOTE: Design flow:

1. Draw the schematic and verify the following
2. DC Analysis
3. AC Analysis
4. Transient Analysis
5. Draw the Layout and verify the DRC, ERC
6. Check for LVS
REAL TIME OPERATING SYSTEMS

Sub. Code 15VDE203
Hrs./Week 4+0+0+1
Total Hrs. 52

CIE Marks 50
SEE Marks 50
Credits 5

Course Outcomes:

At the end of the course the student should be able to:

1. Get a brief introduction to the history of real-time operating systems.
2. Understand basic concepts of scheduling policies.
3. Analyze Scheduling algorithms for better understanding the execution of real time services.
4. Understand memory and I/O architectures of real-time systems for better design.
5. Understand software and hardware challenges faced by a real-time system services to meet deadlines.
6. Get knowledge on embedded system components and debugging components.
7. Understand performance tuning procedures to design better systems.
8. Analyze the high reliability and high availability designs.
9. Perform in depth analysis of real-time systems as a case-study.

UNIT-I


UNIT-II

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies. EDF algorithm, IRIS tasks, Multiprocessor scheduling algorithms.

UNIT-III


Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.

Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.
UNIT-IV

**Embedded System Components**: Firmware components, RTOS system software mechanisms, Software application components.


*(Self Study/Case Study)*: Hardware Synchronization using PLL's, Software Synchronization algorithms (Interactive Convergence Averaging algorithms), Clock and its representations. 10 Hrs

UNIT-V

**Performance Tuning**:

Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

**High availability and Reliability Design**:

Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade offs, Hierarchical applications for Fail-safe design.

**Design of RTOS – PIC microcontroller**. (Chap 13 of book Myke Predko). *(Self Study/Case Study)*: Case studies based on MUCOS, VxWorks such as ACVM, Sending application layer byte streams on TCP/IP stack, Smart card application. 10 Hrs

**Reference Books**:

APPLICATION LAB –II
(VLSI & RTOS)

Sub Code  15VDE204
Hrs./Week  0+0+0+4
CIE Marks  100
SEE Marks  --
Crédits  2

VLSI LAB

TOOLS TO BE USED: CADANCE/SYNOPSIS/MENTOR GRAPHICS.

1. Design a VCO for the given specifications.
2. Design a PLL and measure all the parameters.
3. Design a simple 8-bit DAC and measure the data conversion time.
4. Design successive approximation ADC and determine its characteristics.

Real Time Operating Systems LAB

USE LINUX/SOLARIS/QNX OS ONLY.

1. Implement simple IPC protocol.
2. Implement Semaphore and Mutex for any given applications.
3. Communicate between 2 PCs using Socket programming or message passing techniques (ie., MPI).
4. Create a POSIX based message queue for communicating between several tasks as per the requirements given below:-
   i. Use a named message queue with name „MyQueue‟.
   ii. Create N tasks with stack size 4000 & priorities (n-1) & n respectively. N can be any number but more than 4.
   iii. Tasks creates the specified message queue as Read Write and reads the message present, if any, from the message queue and prints it on the console.
   iv. Tasks open the message queue and posts the message „Hi from Task(n-1)‟.

MINI PROJECTS: (optional)

1. Implement protocol converter (refer book 3 given in the RTOS theory)
2. Implement System Calls for the RTOS using RTLinux.
3. Implement an IP phone.
4. Implement Device Driver.
ELECTIVE-III

ADVANCED MICROCONTROLLER

Sub. Code      15VDE211
Hrs./Week     4+0+0+0
Total Hrs.       52

CIE Marks       50
SEE Marks       50
Credits       5

Course Outcomes:

At the end of the course the student should be able to:

- Use different Microcontrollers (CISC or RISC) in the embedded system design.
- Understand concept of Operating system running on embedded platform.
- Design and manipulate on chip peripherals related to the processor.
- Design embedded system suitable for any small scale application.
- Use different embedded integrated development environment (IDE) and necessary cross Compilers.

UNIT-I

MSP430 – 16-bit Microcontroller family. CPU architecture, Instruction set, Interrupt mechanism, Clock system, Memory subsystem, bus -architecture. 12 Hrs

UNIT-II

The assembly language and C programming for MSP-430 microcontrollers. 10 Hrs

UNIT-III

On-chip peripherals. WDT, Comparator, Op-Amp, Timer, Basic Timer, Real Time Clock (RTC), ADC, DAC, Digital I/O. Using the low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and interrupts. 10 Hrs

UNIT-IV


UNIT-V

Applications – Wireless Sensor Networking with MSP430 and Low-Power RF circuits; Pulse Width Modulation(PWM) in Power Supplies. 6 Hrs
References Books:

R4. Sample Programs for MSP430 downloadable from msp430.com
ALGORITHMS FOR VLSI

Sub. Code          15VDE212       CIE Marks  50
Hrs./Week          4+0+0+0       SEE Mark   50
Total Hrs.         52             Credits   4

UNIT-I

Graph Algorithms: Graph search Algorithms, Spanning tree Algorithm, Shortest path Algorithm, Matching Algorithm, Min cut and Max cut Algorithms and Steiner Tree Algorithm. 10 Hrs

UNIT-II

Computational geometry Algorithms: Line sweep method and extended line sweep method.

Basic data structures: Linked list of blocks, Bin based method, neighbor pointers and corner stitching.

Graph Algorithms for physical design: Classes of graphs in physical design, relationship between graph classes, graph problems, Algorithms for interval graphs and Algorithms for permutations graphs. 10 Hrs

UNIT-III

Partitioning: Group migration Algorithms.

Floor planning and Pin assignment: floor planning, chip planning and pin assignment. 10 Hrs

UNIT-IV

Placement: Simulated annealing, simulated evolutions, force directed placement, sequence pair technique, Breuer’s Algorithm, Terminal propagation Algorithm, Cluster growth and quadratic assignment. 10 Hrs

UNIT-V


Over the cell routing, Via minimization, clock, power and ground routing. 12 Hrs

Reference books:


LOW POWER VLSI DESIGN

Sub. Code 15VDE213  
CIE Marks 50

Hrs./Week 4+0+0+0  
SEE Marks 50

Total Hrs. 52  
Credits 4

UNIT-I

Introduction: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation 12 Hrs

UNIT-II

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Monte Carlo simulation. 10 Hrs

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. 10 Hrs

UNIT-III

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic 10 Hrs

UNIT-IV

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

UNIT-V

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network 10 Hrs

Reference Books:
ELECTIVE-IV
SYSTEM DESIGN USING EMBEDDED PROCESSORS

Sub. Code  15VDE221  CIE Marks  50
Hrs./Week  4+0+0+0  SEE Marks  50
Total Hrs.  52  Credits  4

UNIT-I

8-Bit Microcontrollers:
Architecture: CPU Block diagram, Memory Organization, Program memory, Data Memory, Interrupts
Peripherals: Timers, Serial Port, I/O Port
Programming: Addressing Modes, Instruction Set, Programming
Microcontroller based System Design:
Timing Analysis
Case study with reference to 8-bit 8051 Microcontroller.
A typical application design from requirement analysis through concept design, detailed hardware and software
design using 8-bit 8051 Microcontrollers. 12 Hrs

UNIT-II

32- Bit ARM920T Processor Core:
Introduction: RISC/ARM Design Philosophy, About the ARM920T Core, Processor Functional Block Diagram
Programmers Model: Data Types, Processor modes, Registers, General Purpose Registers, Program Status
Register, CP15 Coprocessor, Memory and memory mapped I/O, Pipeline, Exceptions, Interrupts and Vector table,
Architecture revisions, ARM Processor Families.
Cache: Memory hierarchy and cache memory,
Cache Architecture – Basic Architecture of a Cache, Basic operation of a cache controller,
Cache and main memory relationship, Set Associativity, Cache Policy – Write policy, Cache line replacement
policies, allocation policy on a cache miss Instruction Cache, Data Cache, Write Buffer and Physical Address TAG
RAM
Memory Management Units: How virtual memory works, Details of the ARM MMU, Page Tables,
Translation Look-aside Buffer Domains and Memory access permissions 10 Hrs

UNIT-III

ARM Instruction Set: Data Processing instructions, Branch instructions, Load - Store instructions,
Software Interrupt Instruction, Program Status Register Instruction, Loading Constants
Thumb Instruction Set: Thumb register usage, ARM-Thumb interworking, Branch instruction,
Data processing instructions, Load-store instructions, stack instructions, software interrupt instructions.

**Interrupt Handling:** Interrupts, Assigning interrupts, Interrupt latency, IRQ & FIQ exceptions,
Basic interrupt stack design, and implementation, Non-nested Interrupt handler

**UNIT-IV**

**ARM9 Microcontroller Architecture:**
AT91RM9200 Architecture: **Block Diagram, Features, Memory Mapping**
**Memory Controller (MC),** Memory Controller Block Diagram, Address Decoder, External Memory Areas,
Internal Memory Mapping
**External Bus Interface (EBI),** Organization of the External Bus Interface, EBI Connections to
Memory Devices
**External Memory Interface,** Write Access, Read Access, Wait State Management
AT91RM9200 PERIPHERALS
**Interrupt Controller:** Normal Interrupt, Fast Interrupt, AIC
**System Timer (ST):** Period Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT)
**Real Time Clock (RTC)**
Parallel Input/Output Controller (PIO)

**UNIT-V**

**Development & Debugging Tools for Microcontroller based Embedded Systems:**
Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE),
Logic Analyzer etc.

Reference Books:

R1. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and
Optimizing System Software”, Elsevier, 2006
MEMS AND IC INTEGRATION

Sub. Code 15VDE222
Hrs./Week 4+0+0+0
Total Hrs. 52
CIE Marks 50
SEE Marks 50
Credits 4

Course Outcomes:

At the end of the course the student should be able to:

1. Design mask for given structure
2. Decide the process flow for given structure
3. Understand the micro-fabrication techniques
4. Understand various signal conditioning circuits for enhancing the sensed data.
5. Understand working principle, circuit integration and signal conditioning of standard MEMS sensors
6. Understand the scaling issues

UNIT I
Overview of CMOS process in IC fabrication – Crystal growth, doping, Growth and deposition of dielectric layers, epitaxial growth, masking and photolithography, etching, metallization, surface and bulk micromachining, LIGA process, wafer bonding. 12 Hrs

UNIT II
MEMS system-level design methodology, Equivalent Circuit representation of MEMS, signal-conditioning circuits, and sensor noise calculation. 10 Hrs

UNIT III
Pressure sensors with embedded electronics (Analog/Mixed signal), Accelerometer with transducer, Gyroscope, Bolo meter 10 Hrs

UNIT IV
RF MEMS, Optical MEMS 10 Hrs

UNIT V
MEMS scaling issues 10 Hrs

Reference Books:

VLSI SIGNAL PROCESSING

Sub. Code   15VDE223  CIE Marks   50
Hrs./ week  4+0+0+0  SEE Marks   50
Total Hrs.  52  Credits   4

UNIT-I

Introduction to DSP systems – Data flow representations - Iteration Bound – Pipelined and parallel processing. 12 Hrs

UNIT-II

Retiming – unfolding – algorithmic strength reduction in filters and transforms. 10 Hrs

UNIT-III

Systolic architecture design – fast convolution – pipelined and parallel recursive and adaptive filters. 10 Hrs

UNIT-IV

Scaling and round off noise – digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic. 10 Hrs

UNIT-V

Numerical strength reduction – synchronous, wave and asynchronous pipelines – low power design – programmable digit signal processors & applications. 10 Hrs

Reference Books: