NMAM INSTITUTE OF TECHNOLOGY
(An Autonomous Institution under VTU, Belgaum)

Syllabus of
Master of Technology
in
DIGITAL ELECTRONICS & COMMUNICATION
Effective from 2014-2015

Department of
Electronics and Communication Engineering
## SCHEME OF TEACHING AND EXAMINATION FOR
M.TECH. - DIGITAL ELECTRONICS & COMMUNICATION - 2014 SCHEME

### I SEMESTER

<table>
<thead>
<tr>
<th>Sub. code</th>
<th>Name of the Subject</th>
<th>L+T+P+S</th>
<th>Self study /Case Study Hrs/ Week</th>
<th>Contact Hrs/week</th>
<th>Duration of Sem End Exam in hours</th>
<th>Marks for</th>
<th>Total Credits</th>
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<td>Application Laboratory-I (Experiments on 14DEC102 &amp; 14DEC103)</td>
<td>0+0+4+0</td>
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**TOTAL:** 20+4+4+4  4  28  15  350  250  25

### ELECTIVE – I

- 14DEC111 Synthesis & Optimization of Digital Circuits
- 14DEC112 Linear Algebra
- 14DEC113 Optical Communication & Networking
- 14DEC114 Speech & Audio Processing

### ELECTIVE – II

- 14DEC121 Advanced Computer Networks
- 14DEC122 Mixed Signal VLSI Design
- 14DEC123 Digital Signal Compression
- 14DEC124 RF & Microwave Design
## II SEMESTER

<table>
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<th>L+T+P+S</th>
<th>Self study / Case Study Hrs/Week</th>
<th>Contact Hrs/week</th>
<th>Duration of Sem. End Exam in hours</th>
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<td>Advances in VLSI Design</td>
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### ELECTIVE – III
- 14DEC211  Advanced Computer Architecture
- 14DEC212  Image & Video Processing
- 14DEC213  Pattern Recognition
- 14DEC214  Wireless & ATM Networks

### ELECTIVE - IV
- 14DEC221  Cryptographic Systems
- 14DEC222  Detection & Estimation
- 14DEC223  Error Control Coding
- 14DEC224  VLSI Systems & Architecture
### III SEMESTER

<table>
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<th>Sub. code</th>
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<th>Marks for Practical/Field work/Assignment</th>
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<td>Industrial Training/Mini-Project</td>
<td>Full time 8 weeks</td>
<td>100</td>
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<tr>
<td>14DEC302</td>
<td>Seminar on special topics</td>
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<tr>
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<td>Project-part I</td>
<td>Full time 8 weeks</td>
<td>200</td>
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### IV SEMESTER

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<th>Duration</th>
<th>Marks for Practical/Field work work</th>
<th>Total Credits</th>
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<tr>
<td>14DEC401</td>
<td>Project –part II Report Submission, Evaluation &amp; Viva-voce</td>
<td>14 weeks 4 weeks</td>
<td>100 Report = 100 Viva-voce=200</td>
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| TOTAL     |                                         | 100 300                | 30                                  |

GRAND TOTAL from 1<sup>st</sup> to 4<sup>th</sup> semester : 100 credits

**Note:**

1. **14DEC301**: Industrial Training /mini-project: Practical training report and oral presentation are to be evaluated by the Department Committee for 50 marks each. Alternatively, if mini-project is carried out, it is evaluated for 100 marks by the Department.

2. **14DEC302**: The Seminar Marks are to be awarded by the Department Committee constituted for the purpose.

3. **14DEC303**: Progress of work to be assessed by the Department Committee including the guide for 100 marks.

4. **14DEC401**: The project report valuation will be carried out separately by the guide for 50 marks, Department Committee for 50 marks (total IA marks 100) and the external examiner for 100 marks. Viva-Voce will carry 200 marks and will be conducted by a committee consisting of the following:
   - (a) Chairman, BOE (PG) or his nominee,
   - (b) Project Guide and External Examiner
ADVANCED EMBEDDED SYSTEMS

Subject Code: 14DEC101  
Credits: 5

Hours/Week: 4+0+0+4  
CIE: 50 Marks

Total Hours: 52  
SEE: 50 Marks

UNIT-I
8 Hrs

UNIT-II
10 Hrs

UNIT-III
Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages, Programming in Embedded C  
12 Hrs

UNIT-IV
Real-Time Operating System (RTOS) based Embedded System Design:  
Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS (Self Study/Case Study).  
12 Hrs

UNIT-V
The Embedded System Development Environment: The Integrated Development Environment (IDE) (Self Study/Case Study), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Trends in the Embedded Industry: (Self Study/Case Study), Processor Trends in Embedded Systems, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks.  
10 Hrs

Reference Books:
ADVANCED SIGNAL PROCESSING

Subject Code 14DEC102  Credits  5
Hours/Week 4+2+0+0  CIE  50 Marks
Total Hours 52  SEE  50 Marks

UNIT-I


UNIT-II

Adaptive Filters: Principles of Adaptive Filters, Tapped delay line filters, LMS and RLS Algorithms
Application of Adaptive Filters: Noise Canceller, Echo Canceller, Side Lobe Canceller, Adaptive Line Enhancer. 10 Hrs

UNIT-III

Orthogonal Transforms: Fourier Representation, Two –dimensional DFT, Time varying frequency spectra, Class of Orthogonal functions
Rademacher, Haar and Walsh Functions, Walsh – Hadamard Transformation, Spectra, Cyclic and Dyadic Correlation and Convolution. 10 Hrs

UNIT-IV

Generalized Weiner Filtering, Mathematical model, Filter design, Optimal and Sub-optimal filter 10 Hrs

UNIT-V


Reference Books:
ADVANCED DIGITAL COMMUNICATION

Subject Code 14DEC103
Credits 5
Hours/Week 4+2+0+0
Total Hours 52

UNIT-I
Review of Digital Modulation Techniques, Optimum Receiver for Signals Corrupted by AWGN, Concept of matched filter. 6 Hrs

UNIT-II
Coding Techniques: Convolutional Codes, Hamming Distance Measures for Convolutional Codes; Maximum Likelihood Decoding of Convolutional codes, Sequential Decoding and Feedback Decoding, Viterbi decoding Soft Decision, Trellis Coded Modulation 10 Hrs

UNIT-III
Communication through band limited linear filter channels: Optimum receiver for channels with ISI and AWGN, Linear equalization, Decision-feedback equalization, reduced complexity ML detectors, Iterative equalization and decoding-Turbo equalization.

Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer, adaptive equalization of Trellis coded signals, Recursive least squares algorithms for adaptive equalization. 12 Hrs

UNIT-IV

UNIT-V
Digital Communication through fading multi-path channels: Characterization of fading multi-path channels, the effect of signal characteristics on the choice of a channel model, frequency-Nonselective, slowly fading channel, diversity techniques for fading multi-path channels, Digital signal over a frequency selective, slowly fading channel, coded wave forms for fading channels. 12 Hrs

Reference Books:
APPLICATION LAB -I

<table>
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<th>CIE</th>
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Hours/Week: 0+0+0+4

Advanced Digital Communication

1. 8-PSK Modulation
2. QPSK DSSS
3. MSK Modulation
4. Analog TDM
5. Study of PLL (PLL characteristics & FSK Demodulation)

Advanced Signal Processing

1. LMS Algorithm
2. ARMA Model
3. MA Model
4. Recursive Algorithm
SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Subject Code 14DEC111  Credits 4
Hours/Week 4+0+0+0  CIE 50 Marks
Total Hours 52  SEE 50 Marks

UNIT-I
Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization. 10 Hrs

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.

UNIT-II
Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.
Schedule Algorithms: A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits. 10 Hrs

UNIT-III
Two level combinational logic optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations. 10 Hrs

UNIT-IV
Multiple level combinational optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization. 10 Hrs

UNIT-V
Sequential circuit optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.
Cell library binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding. 12 Hrs

Reference Books:
LINEAR ALGEBRA

Subject Code 14DEC112
Credits 4
Hours/Week 4+0+0+0
CIE 50 Marks
Total Hours 52
SEE 50 Marks

UNIT-I

Linear equations: Field, System of linear equations and its solution sets, Elementary row operations and echelon forms, Matrix operations, Invertible matrices, LU factorization of a matrix. 10 Hrs

UNIT-II

Vector spaces: Vector spaces and subspaces, Null spaces, Column spaces & Linear transformation, Linearly independent sets, Bases, Linear combinations, spanning set theorem, Coordinate systems, Dimension of a vector space, Rank, Change of basis. 10 Hrs

UNIT-III

Linear Transformations: Linear transformations, Matrix transformations, algebra of linear transformations, isomorphism, representation of transformations by matrices; linear functional. 6 Hrs
Canonical Forms: Characteristic values, Characteristic equation, Minimal polynomial, Characteristic & Minimal polynomials of block matrices, Invariant direct-sum decompositions, primary decomposition theorem, cyclic subspaces, Jordan Canonical form. 6 Hrs

UNIT-IV

Inner Product Spaces: Inner products, Examples of inner product spaces, Cauchy-Schwarz inequality, orthogonal sets and projections, Gram-Schmidt process of orthogonalization, QR-factorization, Least-squares problems and solutions. 10 Hrs

UNIT-V

Symmetric Matrices and Quadratic Forms: Diagonalization: Characteristic polynomial, Cayley-Hamilton theorem, Eigen values & Eigen vectors, Diagonalization of real symmetric matrix, Quadratic forms, constrained optimization, Singular Value Decomposition. 10 Hrs

Reference Books:
OPTICAL COMMUNICATION & NETWORKING

Subject Code: 14DEC113
Credits: 4

Hours/Week: 4+0+0+0
CIE: 50 Marks

Total Hours: 52
SEE: 50 Marks

UNIT-I

Introduction: Propagation of signals in optical fiber, different losses, nonlinear effects, solitons, optical sources, detectors.

Optical Components: Couplers, isolators, circulators, multiplexers, filters, gratings, interferometers, amplifiers.

10 Hrs

UNIT-II

Modulation — Demodulation: Formats, ideal receivers, Practical detection receivers, Optical preamplifier, Noise considerations, Bit error rates, Coherent detection.

Transmission system engineering: system model, power penalty, Transmitter, Receiver, Different optical amplifiers, Dispersion.

10 Hrs

UNIT-III

Optical networks: Client layers of optical layer, SONET/SDH, multiplexing, layers, frame structure, ATM functions, adaptation layers, Quality of service and flow control, ESCON, HIPPI.

10 Hrs

UNIT-IV

WDM network elements: Optical line terminal optical line amplifiers, optical cross connectors, WDM network design, cost trade offs, LTD and RWA problems, Routing and wavelength assignment, wavelength conversion, statistical dimensioning model.

10 Hrs

UNIT-V

Control and management: network management functions, management frame work, Information model, management protocols, layers within optical layer performance and fault management, impact of transparency, BER measurement, optical trace, Alarm management, configuration management. Suitable number of Assignments / Tutorials can be given based on the syllabus

12 Hrs

Reference Books:

SYLLABUS FOR M.TECH DIGITAL ELECTRONICS & COMMUNICATION (AUTONOMY) [2014 Scheme]

Syllabus for Speech and Audio Processing

Subject Code: 14DEC114
Credits: 4
Hours/Week: 4+0+0+0
Total Hours: 52

UNIT-I
Digital models for the speech signal: Process of speech production, Acoustic theory of speech production, Lossless tube models, and Digital models for speech signals.

Time domain models for speech processing: Time dependent processing of speech, Short time energy and average magnitude, Short time average zero crossing rate, Speech vs silence discrimination using energy & zero crossings, Pitch period estimation, Short time autocorrelation function, Short time average magnitude difference function, Pitch period estimation using autocorrelation function, Median smoothing.

UNIT-II

Short time Fourier analysis: Linear Filtering interpretation, Filter bank summation method, Overlap addition method, Design of digital filter banks, Implementation using FFT, Spectrographic displays, Pitch detection, Analysis by synthesis, Analysis synthesis systems.

UNIT-III
Homomorphic speech processing: Homomorphic systems for convolution, Complex cepstrum, Pitch detection, Formant estimation, Homomorphic vocoder, linear predictive analysis, Solution of LPC equations, Prediction error signal, Frequency domain interpretation, Relation between the various speech parameters, Synthesis of speech from linear predictive parameters, Applications.


UNIT-IV

Automatic Speech Recognition: Introduction, Speech recognition vs. Speaker recognition, Signal processing and analysis methods, Pattern comparison techniques, Hidden Markov Models, Artificial Neural Networks.

UNIT-V
Audio Processing: Auditory perception and psychoacoustics - Masking, frequency and loudness perception, spatial perception, Digital Audio, Audio Coding -High quality, low-bit-rate audio coding standards, MPEG, AC-3, Multichannel audio - Stereo, 3D binaural and Multichannel surround sound.

Reference Books:
ADVANCED COMPUTER NETWORKS

Subject Code  14DEC121  Credits  4
Hours/Week  4+0+0+0  CIE  50 Marks
Total Hours  52  SEE  50 Marks

UNIT-I
Introduction to computer networks; telephone networks, networking principles; multiple access, multiplexing - FDM, TDM, SM; local area networks - Ethernet, token ring, FDDI;  
10 Hrs

UNIT-II
Switching - circuit switching, packet switching, multicasting;
Scheduling - performance bounds, best effort disciplines, naming and addressing, protocol stack, SONET/SDH;  
10 Hrs

UNIT-III
ATM networks - AAL, virtual circuits, SSCOP; Internet -addressing, routing, end point control; Internet protocols.  
10 Hrs

UNIT-IV
Traffic management - models, classes, scheduling; control of networks - QOS, static and dynamic routing, Markov chains, queuing models, Single queuing systems, Poisson process, Burke’s theorem, M/M/∞ queuing systems, Network of Queues, the global balance equation. Case Study: Queuing on a space division Packet Switch, on a Single buffered Banyan Switch.  
12 Hrs

UNIT-V
Bellman Ford and Dijkstra's algorithms, window and rate congestion control, large deviations of a queue and network, open and closed loop flow control, control of ATM networks.  
10 Hrs

Reference Books:
R5. Anurag Kumar, Joy Kurien, “Advanced Computer Networks”
MIXED SIGNAL VLSI DESIGN

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<th>Credits</th>
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**UNIT-I**
Introduction to CMOS analog circuits, MOS transistor DC and AC small signal parameters from large signal model, Common source amplifier with resistive load, diode load and current source load, Source follower, Common Gate amplifier, Cascode amplifier, folded cascade amplifier, Frequency response of amplifiers. 12 Hrs

**UNIT-II**
Current source/sink and mirror circuits, Wilson current source and regulated cascade current source, Band gap references.
Differential amplifiers, Gilbert cell, Op-amps, Design of two stage op-amp, DC and AC response, Frequency compensation, slew rate, Offset effects, PSRR, Noise. 12 Hrs

**UNIT-III**
Comparators, Sense amplifier, Sample and hold, sampled data circuits, Switched capacitor filters.
Data converters: Fundamentals, Characteristics, architectures of DAC and ADC. 15 Hrs
RF amplifiers, Oscillators, PLL and Mixer.

Reference Books:
DIGITAL SIGNAL COMPRESSION

Subject Code 14DEC123
Credits 4
Hours/Week 4+0+0+0
CIE 50 Marks
Total Hours 52
SEE 50 Marks

UNIT-I
Introduction: Compression techniques, Modeling & coding, Distortion criteria, Differential Entropy, Rate Distortion Theory, Vector Spaces, Information theory, Models for sources, Coding – uniquely decodable codes, Prefix codes, Kraft McMillan Inequality 8 Hrs

UNIT-II
Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ – Gain shape VQ, Mean removed VQ, Classified VQ, Multistage VQ, Adaptive VQ, Trellis coded quantization 10 Hrs

UNIT-III
Transform Coding: Transforms – KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression – JPEG, Application to audio compression. 10 Hrs

UNIT-IV
Analysis/Synthesis Schemes: Speech compression – LPC-10, CELP, MELP, Image Compression – Fractal compression. 12 Hrs

UNIT-V

Reference Books:
RF AND MICROWAVE CIRCUIT DESIGN

Subject Code 14DEC124  
Credits 4  
Hours/Week 4+0+0+0  
Total Hours 52

CIE 50 Marks
SEE 50 Marks

UNIT-I
Wave Propagation in Networks: Introduction to RF/Microwave Concepts and applications; RF Electronics Concepts; Fundamental Concepts in Wave Propagation; Circuit Representations of two port RF/MW networks

10 Hrs

UNIT-II

10 Hrs

UNIT-III
Basic Considerations in Active Networks: Stability Consideration in Active networks, Gain Considerations in Amplifiers, Noise Considerations in Active Networks.

10 Hrs

UNIT-IV

12 Hrs

UNIT-V

10 Hrs

Reference Books:

**ADVANCES IN VLSI DESIGN**

**Subject Code** 14DEC201  
**Credits** 5  
**Hours/Week** 4+0+0+4  
**Total Hours** 52

**CIE** 50 Marks  
**SEE** 50 Marks

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**UNIT- I**

**Review of MOS Circuits:** MOS and CMOS static plots, CMOS switches  
**System Design:** CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, programmable structure, standard cell approach, Full custom Design, Gate arrays (Self Study/Case Study), Programmable inter connect (Self Study/Case Study)  
**MESFET and MODFETs:** Structure, operations, quantitative description of MESFETS.  
6 Hrs

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**UNIT-II**

**MIS Structures and MOSFETS:** MIS systems in equilibrium, under bias, small signal operation of MESFETS and small signal analysis of MOSFETS (Self Study/Case Study).  
4 Hrs

**Super Buffers:** NMOS super buffers, NMOS tri-state super buffer and pad drivers, CMOS super buffers, RC delay lines (Self Study/Case Study)  
6 Hrs

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**UNIT-III**

**Short Channel Effects:** Two dimensional Potential profile, High electric field in the short channel, Punch-through and channel length modulation.  
6 Hrs

**Steering Logic:** Driving large capacitive loads, pass-transistor logic, designing pass-transistor logic, Dynamic ratio less inverters, General functional blocks - NMOS and CMOS functional blocks.  
5 Hrs

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**UNIT-IV**

**Scaling Theory:** Constant filed, constant voltage and quasi-constant voltage models  
**Beyond CMOS:** Evolutionary advances beyond CMOS: SOI MOSFET  
4 Hrs

Revolutionary advances beyond CMOS: carbon Nano-tubes, Conventional vs. tactile computing, molecular and biological computing.

Molectronics-Molecular Diode and diode- diode logic  
5 Hrs

Defect tolerant computing (Self Study/Case Study).

**Challenges to CMOS:** Processing Challenges to Further CMOS Miniaturization (Self Study/Case Study).

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**UNIT-V**

**Special Circuit Layouts and Technology Mapping:** Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logics, NMOS, CMOS Multiplexers, Barrel shifter.  
7 Hrs

Wire routing Algorithms: Need for algorithms, study of Lee-Moore Maze running algorithm and line search algorithm.  
5 Hrs
Reference Books:


MULTIRATE SYSTEMS AND FILTER BANKS

Subject Code 14DEC202 Credits 5
Hours/Week 4+2+0+0 CIE 50 Marks
Total Hours 52 SEE 50 Marks

UNIT-I
Fundamentals of Multi-rate Systems: Basic multi-rate operations, interconnection of building blocks, poly-phase representation, multistage implementation, applications of multi-rate systems, special filters and filter banks.

10 Hrs

UNIT-II
Multirate Filter Banks: Maximally decimated filter banks: Errors created in the QMF bank, alias-free QMF system, power symmetric QMF banks, M-channel filter banks, poly-phase representation, perfect reconstruction systems, alias-free filter banks, tree structured filter banks, trans-multiplexers.

10 Hrs

UNIT-III
Para-unitary Perfect Reconstruction Filter Banks: Lossless transfer matrices, filter bank properties induced by paraunitariness, two channel Para-unitary lattices, M-channel FIR Para-unitary QMF banks, transform coding.

10 Hrs

UNIT-IV
Linear Phase Perfect Reconstruction QMF Banks: Necessary conditions, lattice structures for linear phase FIR PR QMF banks, formal synthesis of linear phase FIR PR QMF lattice.

10 Hrs

UNIT-V
Cosine Modulated Filter Banks: Pseudo-QMF bank and its design, efficient poly-phase structures, properties of cosine matrices, cosine modulated perfect reconstruction systems.

Wavelet Transform: Short-time Fourier transform, Wavelet transform, discrete-time Ortho-normal wavelets, continuous time Ortho-normal wavelets.

12 Hrs

Reference Books:
ADVANCED WIRELESS COMMUNICATION

Subject Code: 14DEC203

Credits: 5

Hours/Week: 4+2+0+0

Total Hours: 52

CIE: 50 Marks

SEE: 50 Marks

UNIT-I

Cellular Concept: Cellular concept fundamentals, frequency reuse, channel assignment strategies, handoff, trunking and grade of service, improving coverage and capacity. 10 Hrs

UNIT-II

Diversity Techniques: Introduction and Principle of diversity, Types, Combining and switching methods, Rake receiver, Transmit and Receive diversity, Space time coding – Alamouti codes design and properties, BLAST architectures, MIMO systems. 10 Hrs

UNIT-III

CDMA Systems: Introduction to CDMA, Direct Sequence CDMA, Frequency Hop CDMA, Pulse position hopped CDMA, Orthogonal and Quasi-orthogonal expansions of Spread spectrum signals, Reception of Spread Spectrum signals in AWGN channel - Introduction to Block Coding, First-Order Reed–Muller Code, Noncoherent Reception of Encoded DS CDMA Signals, Introduction to Convolutional Coding, Convolutional Coding in DS CDMA Systems, Orthogonal Convolutional Codes, Coding in FH and PPH CDMA Systems, Concatenated Codes in CDMA Systems, Forward Error Control Coding in Spread Spectrum. 10 Hrs

UNIT-IV

OFDM: Introduction, Principle of OFDM, Frequency selective channels, Channel estimation, Peak to average power ratio, Intercarrier interference, Adaptive modulation and capacity, Multiple access, Impairment of wireless channels to OFDM. 10 Hrs

UNIT-V

UWB: Introduction To Ultra-Wideband, Ultra-wideband application classes, Brief history of ultra-wideband, Next generation HDR applications, Matching of UWB to HDR applications, Physical layer characteristics – Multiband, Multiband OFDM.

Ultra-Wideband Channel Modeling:

Principles and Background of UWB Multipath Propagation Channel Modeling - Channel Sounding Techniques - UWB Statistical-Based Channel Modeling - Impact of UWB Channel on System Design - Potential Benefits of MIMO. 10 Hrs

Reference Books:

APPLICATION LAB – II

<table>
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<th>Subject Code</th>
<th>14DEC204</th>
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<tr>
<td>Hours/Week</td>
<td>0+0+0+4</td>
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<td>CIE</td>
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VLSI LAB

1. V-I characteristics of enhancement and depletion mode MOSFETs
2. Schematic simulation of NMOS active load Inverter and CMOS inverter
3. Design and verification of given logic function using pass transistor logic.
4. Design & Simulation of Single stage amplifiers
5. Design & Simulation of differential amplifiers
7. Layout simulation of Barrel Shifter
8. FPGA implementation of Sequential/Combinational logic networks.

Multirate Systems

1. Two Channel Perfect Reconstruction System
2. Transmultiplexers
3. Multistage Approach to Sampling Rate Conversion
4. Sample Rate Conversion Using Polyphore Structure
ADVANCED COMPUTER ARCHITECTURE

Subject Code  14DEC211  Credits  4
Hours/Week  4+0+0+0  CIE  50 Marks
Total Hours  52  SEE  50 Marks

UNIT-I
Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multifactor and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms. 10 Hrs

UNIT-II
System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network. 10 Hrs

UNIT-III
Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors. 10 Hrs

UNIT-IV
Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines
Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies. 10 Hrs

UNIT-V
Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, and MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, and synchronization. Scalable point -point interfaces: Alpha364 and HT protocols, high performance signaling layer.
Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine checks, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system. 12 Hrs
Reference Books:

R2. Hwan and Briggs, “Computer Architecture and Parallel Processing”, MGH.VLSI
IMAGE AND VIDEO PROCESSING

Subject Code 14DEC212  Credits 4
Hours/Week 4+0+0+0  CIE 50 Marks
Total Hours 52  SEE 50 Marks

UNIT-I
Image Perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision.

10 Hrs

UNIT-II
Image Sampling and Quantization: Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization.

10 Hrs

UNIT-III
Image Representation by Stochastic Models: Introduction, one-dimensional Causal models, AR models, Non-causal representations, linear prediction in two dimensions.
Image Enhancement: Point operations, Histogram modeling, spatial operations, Transform operations, Multispectral image enhancement, false color and Pseudo-color, Color Image enhancement.

12 Hrs

UNIT-IV
Image Analysis & Computer Vision: Spatial feature extraction, Transform features, Edge detection, Boundary Extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification Techniques.

10 Hrs

UNIT-V
Image Data Compression: Introduction, Pixel coding, Predictive techniques, Transform coding, Inter-frame coding, coding of two tone images, Image compression standards.

10 Hrs
Reference Books:


PATTERN RECOGNITION

Subject Code  14DEC213
Credits        4
Hours/Week    4+0+0+0
CIE           50 Marks
Total Hours   52
SEE           50 Marks

UNIT-I
Introduction: Applications of pattern recognition, statistical decision theory, image processing and analysis.
Probability: Introduction, probability of events, random variables, Joint distributions and densities, moments of random variables, estimation of parameters from samples, minimum risk estimators 10 Hrs

UNIT-II
Statistical Decision Making: Introduction, Baye’s Theorem, multiple features, conditionally independent features, decision boundaries, unequal costs of error, estimation of error rates, the leaving-one—out technique. Characteristic curves, estimating the composition of populations. 10 Hrs

UNIT-III
Nonparametric Decision Making: Introduction, histograms, Kernel and window estimators, nearest neighbor classification techniques, adaptive decision boundaries, adaptive discriminate Functions, minimum squared error discriminate functions, choosing a decision making technique. 10 Hrs

UNIT-IV
Clustering: Introduction, hierarchical clustering, partitional clustering
Artificial Neural Networks: Introduction, nets without hidden layers. nets with hidden layers, the back Propagation algorithms, Hopfield nets, an application. 10 Hrs

UNIT-V
Processing of Waveforms and Images: Introduction, gray level sealing transformations, equalization, geometric image and interpolation, Smoothing, transformations, edge detection, Laplacian and sharpening operators, line detection and template matching, logarithmic gray level sealing, the statistical significance of image features. 12 Hrs

Reference Books:
R2. Duda and Hart, “Pattern recognition (Pattern recognition a scene analysis)”
WIRELESS & ATM NETWORKS

Sub. Code : 14DEC214  
CIE : 50 Marks  
Hrs./Week : 4+0+0+0  
SEE : 50 Marks  
Total Hrs. : 52  
Credits : 4

UNIT-I
PCS Architecture, Cellular telephony, Cordless telephony and low tier PCS, Third and Fourth generation wireless systems; Mobility management, handoff, roaming management for SS& and CT2, handoff Detection, strategies for handoff detection, channel assignment, link transfer types, hard Handoff soft handoff.  
10 Hrs

UNIT-II
IS-41 signaling, IS-41 handoff and authentication, CDPD architecture, CDPD air Interface, radio resource allocation.; GSM architecture, location tracking, data services, HSCP, GPRS, OSM network signaling, GSM mobility management, GSM short message service, International Roaming for GSM; VoIP for GSM networks.; GPRS functional groups, architecture, network nodes, interfaces, procedures, billing.  
12 Hrs

UNIT-III
Evolving from GSM to GPRS, WAP protocols, W-CDMA and CDMA 2000, QOS in 3G, paging network architectures, wireless local loop architectures, Bluetooth core Protocols; Introduction to wireless LANS, 802.11 WLANs, physical and MAC layers, Wireless ATM and HIPERLAN, 802.15 WPAN.  
10 Hrs

UNIT-IV
Bluetooth, interference between Bluetooth and 802.11, wireless geolocation system architecture, standards, performance measures, introduction other wireless LAN standards 802.11e, 802.16, 802.17, 802.19, 802.20  
10 Hrs

UNIT-V
Assignments can be given on simulation of mobility management, handoff schemes, wireless MAC protocols and application development over wireless LANs. GlomoSim tool can be used for simulation, which is free software on Linux. Also, student can collect recent articles from magazines/Journals and prepare survey paper or a technical report.  
10 Hrs

Reference Books:
CRYPTOGRAPHIC SYSTEMS

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<tr>
<td>Hours/Week</td>
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UNIT-I

Overview: Services, Mechanisms and attack models, Model for network security, Symmetric cipher model, Substitution techniques, Transposition techniques. *(Self Study: Rotor machine, Steganography.)*

Block Ciphers and DES, Block cipher design principles, Block cipher modes of operation. Differential and Linear cryptanalysis 3DES, Rijndael system, AES, IDEA

9 Hrs+ (SS=3 Hrs)

UNIT-II


10 Hrs

UNIT-III

Other Public Key Crypto Systems and Key Management: Key management, Diffie-Hellman key exchange, DH with multiple participants, Elliptic curve arithmetic, Elliptic curve cryptography, Analog of Massey –Omura, Analog of ElGamal crypto systems. Elliptic curve factorization - pollard’s p-1 method, Lenstra’s elliptic curve factorization algorithm, Hyper elliptic curve cryptography.

10 Hrs

UNIT-IV

Message Authentication and Hash Functions: Authentication requirements, Authentication functions, Message authentication codes, Hash functions, Security of hash functions and MAC.

Digital Signature and Authentication Protocol: Digital signature, Authentication protocols, Digital signature standard, RSA digital signatures, ElGamal digital signatures and DSA, ECDSA

8 Hrs

UNIT-V

Zero-knowledge proofs, Secret sharing schemes, Identification schemes.

2 Hours + (SS=10 Hrs)

*(Self Study: SHA-256, SHA-512 and SHA-n.)*

*(Self Study: Introduction to quantum cryptology: Quantum Bit, Quantum Registers and Quantum Algorithm, Shor’s Algorithm, Quantum Key-Exchange.)*

Reference Books:


R6. Keijo Ruohonen, “Mathematical Cryptology” (Translation by Jussi Kangas and Paul Coughlan) -2010
DETECTION AND ESTIMATION

Subject Code  14DEC222  Credits  4
Hours/Week  4+0+0+0  CIE  50 Marks
Total Hours  52  SEE  50 Marks

UNIT-I
10 Hrs

UNIT-II
10 Hrs

UNIT-III
12 Hrs

UNIT-IV
Estimation of Continuous Waveforms: Introduction, derivation of estimator equations, lower bound on the mean-square estimation error, multidimensional waveform estimation, nonrandom waveform estimation.  
10 Hrs

UNIT-V
10 Hrs

Reference Books:
ERROR CONTROL CODING

Subject Code  14DEC223  Credits  4
Hours/Week  4+0+0+0  CIE  50 Marks
Total Hours  52  SEE  50 Marks

UNIT-I
Introduction to Algebra: Groups, Fields, Binary Field Arithmetic, Construction of Galois Field GF (2m) and its basic properties, Computation using Galois Field GF (2m) Arithmetic, Vector spaces and Matrices.
Linear Block Codes: Generator and Parity check Matrices, Encoding circuits, Syndrome and Error Detection, Minimum Distance Considerations, Error detecting and Error correcting capabilities, Standard array and Syndrome decoding, Decoding circuits, Hamming Codes, Reed – Muller codes, The (24, 12) Golay code, Product codes and Interleaved codes. 10 Hrs

UNIT-II
Cyclic Codes: Introduction, Generator and Parity check Polynomials, Encoding using Multiplication circuits, Systematic Cyclic codes – Encoding using Feed back shift register circuits, Generator matrix for Cyclic codes, Syndrome computation and Error detection, Meggitt decoder, Error trapping decoding, Cyclic Hamming codes, The (23, 12) Golay code, Shortened cyclic codes. 10 Hrs

UNIT-III
BCH Codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field Arithmetic, Implementation of Error correction. Non – binary BCH codes: q – ary Linear Block Codes, Primitive BCH codes over GF (q), Reed – Solomon Codes, Decoding of Non – Binary BCH and RS codes: The Berlekamp – Massey Algorithm. 10 Hrs

UNIT-IV
Convolutional Codes: Encoding of Convolutional codes, Structural properties, Distance properties, Viterbi Decoding Algorithm for decoding, Soft – output Viterbi Algorithm, Stack and Fano sequential decoding Algorithms, Majority logic decoding. 10 Hrs

UNIT-V
Concatenated Codes & Turbo Codes: Single level Concatenated codes, Multilevel Concatenated codes, Soft decision Multistage decoding, Concatenated coding schemes with Convolutional Inner codes, Introduction to Turbo coding and their distance properties, Design of Turbo codes. Burst – Error – Correcting Codes: Burst and Random error correcting codes, Concept of Interleaving, cyclic codes for Burst Error correction – Fire codes, Convolutional codes for Burst Error correction. 12 Hrs

Reference Books:
SYLLABUS FOR M.TECH DIGITAL ELECTRONICS & COMMUNICATION (AUTONOMY) [2014 Scheme]

VLSI SYSTEMS & ARCHITECTURE

Subject Code 14DEC224
Credits 4
Hours/Week 4+0+0+0
CIE 50 Marks
Total Hours 52
SEE 50 Marks

UNIT-I

Parallel computer Model: State of computing, multiprocessor & multi-computer multivector & SIMD, VLSI Models (Ref. 1: 1.1 - 1.5)

Pipelining and Architecture: Execution pipeline, Benefits and problems of pipelined execution, Hazards of various types of pipeline stalling, concepts of scheduling (Static and dynamic) and forwarding to reduce / minimize pipeline stalls (Ref. 2: 3.1-3.5)

Instruction Set Architecture with example, SPARC. Architecture, VLIW Architecture, Memory Hierarchy Technology, Virtual Memory Technology, (Ref. 1: 4.1 -4.4)

UNIT-II

Pipelining and Superscalar Techniques: Linear and Non-linear pipeline processors, Instruction pipeline design, arithmetic pipeline design, Superscalar and Superpipeline design (Ref. 1: 6.1-6.5)

Advanced pipelining and ILP-data, control and resource dependencies (Ref. 2:4.1-4.2)

UNIT-III

Multiprocessors and Multicomputer: Cache coherence and Synchronization mechanism (Ref. 1: 7.2)

Scalable Multithreaded and Data Flow Architecture (Ref 1: Chapter 9)

Reference Books:
