DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGG

Syllabus and Scheme of Examination

M.Tech. in VLSI DESIGN AND EMBEDDED SYSTEMS

2017-18

Institution

Vision - Pursuing Excellence, Empowering people, Partnering in Community Development.

Mission - To develop NMAM Institute of Technology, Nitte, as Center of Excellence by imparting Quality Education to generate Competent, Skilled and Humane Manpower to face emerging Scientific, Technological, Managerial and Social Challenges with Credibility, Integrity, Ethics and Social Concern.

Department:

Vision Statement:

Empowering people, Partnering in community development and achieving expertise in the field of Electronics and Communication.

Mission Statement:

To impart effective knowledge of state of the art technology in the field of Electronics and Communication that contributes to the socio-economic development and to generate technical manpower with high degree of credibility, integrity and ethical standards by providing vibrant learning environment.

Programme Educational Objectives

PEO1: Pursue successful careers in industry, academia and entrepreneurial ventures in the domain of VLSI Design and Embedded Systems.

PEO2: Identify & apply appropriate Electronic Design Automation (EDA) to solve real time / research problems in VLSI & Embedded Systems domain.

PEO3: Engage in development activity and add value to the socio-economic development of the region.

Programme Outcomes

PO1: Ann ability to independently carry out research / investigation and development work to solve practical problems

PO2: An ability to write and present a substantial technical report / document

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: An ability to function, manage and lead multidisciplinary teams.

SCHEME OF TEACHING AND EXAMINATION FOR M. TECH. VLSI ESIGN AND EMBEDDED SYSTEMS

Revised at the BOS meeting on 19-05-2017

I SEMESTER

Course Code	Name of the Course	Contact hours/week	Duration of Sem. End Exam in hours	Marks for		Total Credits
		L/T/P/S		CIE	SEE	
17VDE101	Embedded System Design	4/0/2/0	3	50	50	5
17VDE102	CMOS VLSI Design	4/0/2/0	3	50	50	5
17VDE103	VLSI Design Verification	4/2/0/0	3	50	50	5
17VDE11X	Elective - I	4/0/0/0	3	50	50	4
17VDE12X	Elective -II	4/0/0/0	3	50	50	4
17VDE104	Research Experience through Practice-I	0/0/4/0	0	100	--	2
TOTAL			15	350	250	25

ELECTIVE –I		ELECTIVE-II	
17VDE111	Modeling of Digital Systems using VHDL	17VDE121	Advanced Digital System Design
17VDE112	High Speeds VLSI Design	17VDE122	DSP Algorithms & Architecture
17VDE113	SoC Design	17VDE123	Soft Computing
17VDE114	ASIC Design	17VDE124	Synthesis and optimization of Digital Circuits

II SEMESTER

Course Code	Name of the Course	Teaching hours/week	Duration of Sem. End Exam in hours	Marks for		Total Credits
		L/T/P/S		CIE	SEE	
17VDE 201	Advances in VLSI Design	4/0/2/0	3	50	50	5
17VDE 202	Design of Analog VLSI Circuits	4/0/2/0	3	50	50	5
17VDE 203	Real Time Operating Systems	4/0/2/0	3	50	50	5
17VDE 21X	Elective - III	4/0/0/0	3	50	50	4
17VDE 22X	Elective -IV	4/0/0/0	3	50	50	4
17VDE 204	Research Experience through Practice-II	0/0/4/0	0	100	--	2
TOTAL			15	350	250	25

ELECTIVE –III		ELECTIVE - IV	
17VDE211	Advanced Computer Architecture	17VDE221	System Design Using Embedded Processors
17VDE212	Algorithms for VLSI	17VDE222	MEMS and IC Integration
17VDE213	Low Power VLSI Design	17VDE223	VLSI Signal Processing
17VDE214	Nanotechnology	17VDE224	CMOS RF Circuit Design

List of Audit courses currently offered:

LabVIEW Basics

M.TECH. VLSI ESIGN AND EMBEDDED SYSTEMS
(AUTONOMOUS SCHEME)

III SEMESTER

Revised at the BOS meeting on **19-05-2017**

Course Code	Name of the Course	Duration	Marks for		Total Credits
		Practical/Field Work/Assignment	CIE	SEE	
17VDE 301	Industrial Training Mini-Project	Full time 8 weeks	50 (report) 50 (presentation)	--	8
17VDE 302	Seminar on special topics	----	100	--	2
17VDE303	Project-Part I	Full time 10 weeks	100 (report) 100(presentation)	--	10
TOTAL			400		20

IV SEMESTER

Course Code	Name of the Course	Duration	Duration of Exam in Hrs.	Marks for		Total Credits
		Practical Field work		CIE	SEE	
17VDE 401	Project -Part II	Full time 20 weeks		200 [PPE*-I – 100 PPE-II – 100]	200	30
TOTAL				400		30
GRAND TOTAL From 1st to 4th semester: 100 credits (2000 marks)						

PPE* – Project Progress Evaluation

I – SEMESTER

EMBEDDED SYSTEM DESIGN

Course Code	**17VDE101**	**Credits**	**5**
Hours/Week	**4+0+2+0**	**CIE**	**50 Marks**
Total Hours	**52**	**SEE**	**50 Marks**

Course Outcomes:

At the end of the course the student should be able to:

1. Get an insight to the fundamentals and know the general structure of an Embedded System.
2. Understand the Hardware/Software Co-Design involved in an Embedded System.
3. Identify problems and design challenges involved in an Embedded System and program using Embedded C.
4. Understand how RTOS is involved in Embedded System Design.
5. Learn IDE and understand the new trends in embedded industry.

UNIT-I

Typical Embedded System: Core of the Embedded System, Embedded Systems Vs General Computing Systems Memory, Sensors and Actuators, Communication Interface, On Board and External Communication Embedded Firmware, Other System Components.

8 Hrs

UNIT-II

Characteristics and Quality Attributes with Introduction to Hardware software Co-Design:

Characteristics and Quality Attributes ,Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language**,** Hardware Software Trade-offs.

10 Hrs

UNIT-III

Embedded Firmware and Programming Embedded Systems in C: Embedded Firmware Design Approaches, Embedded Firmware Development Languages , Programming in Embedded C using Function Calls, Pointers, Structures, Register Allocation, Conditional Execution and Loops .

12 Hrs

UNIT-IV

Real-Time Operating System (RTOS) based Embedded System Design:

Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS.

12 Hrs

UNIT-V

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.

Trends in the Embedded Industry: Processor Trends in Embedded Systems, Embedded OS Trends, Development Language Trends, Open Standards, Frameworks and Alliances, Bottlenecks.

10 Hrs

Reference Books:

R1. Shibu K V, **"Introduction to Embedded Systems"**, Tata McGraw Hill Education Private Limited, 2009.

R2. James K Peckol, **"Embedded Systems - A Contemporary Design Tool"**, John Wiley, 2008.

LIST OF EXPERIMENTS FOR EMBEDDED SYSTEM DESIGN LAB :

1. Write a C code to interface input device (Keyboard), with output devices (seven segment LED's and free running LEDs) and display the contents of the key pressed on the output.

2. Design a low pass FIR Filter using simulink blocksets.

2. Verilog/VHDL File Processing (Reading a file and storing data in a file).

3. Verilog/ VHDL LCD Display (Scrolling blinking etc.).

CMOS VLSI DESIGN

Course Code	**17VDE102**	**Credits**	**5**
Hours/Week	**4+0+2+0**	**CIE**	**50 Marks**
Total Hours	**52**	**SEE**	**50 Marks**

Course Outcomes:

At the end of the course the student should be able to:

Course Outcomes:

At the end of the course the student should be able to:

1. Explain MOSFET structure, I-V characteristics, drain current equation and second order effects.
2. Explain CMOS process technology, technology scaling, physical design of CMOS circuits.
3. Design MOS Combinational and sequential circuits
4. Design dynamic logic circuits, design CMOS circuits for driving large capacitive load.
5. Explain clocking in CMOS circuits.

UNIT-I

MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. Mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, tristate inverter, BiCMOS inverter.

10 Hrs

UNIT-II

CMOS Process Technology: Semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD, refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits. **10 Hrs**

UNIT-III

Basics of Digital CMOS Design: Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, CMOS full adder, Transmission Gate.

Sequential MOS logic Circuits – Introduction, Behavior of bi-stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and edge triggered Flip Flop.

10 Hrs

UNIT-IV

Dynamic Logic Circuits – Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuits techniques, Dynamic CMOS circuit techniques

Sheet resistance & standard unit capacitance concepts, delay unit time, inverter delays , driving capacitive loads, propagate delays. **12 Hrs**

UNIT-V

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS., Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements.

10 Hrs

Reference Books:

R1. Neil Weste and K. Eshragian, **"Principles of CMOS VLSI Design: A System Perspective"**, Pearson Education (Asia) Pvt. Ltd., 2nd Edition ,2000.

R2. Wayne Wolf, **"Modern VLSI design: System on Silicon"** Pearson Education, Second Edition, 1998

R3. Douglas A Pucknell & Kamran Eshragian , **"Basic VLSI Design"** PHI 3rd Edition (original Edition – 1994)

R4. Sung Mo Kang & Yosuf Leblebici, **"CMOS Digital Integrated Circuits: Analysis and Design"**, McGraw- Hill, 3rd Edition, 2003

CMOS VLSI DESIGN LAB

(Use any of the EDA Tools)

List of Experiments

1. V-I characteristics of NMOSFET
2. Schematic simulation of CMOS Inverter, analysis of the effect of MOSFET sizing on the inverter midpoint voltage.
3. Layout simulation for a CMOS inverter
4. Schematic simulation of area efficient full adder
5. Schematic simulation of transmission gate
6. Schematic simulation of D flip-flop
7. Schematic simulation domino CMOS circuits

VLSI DESIGN VERIFICATION

Course Code	**17VDE103**	**CIE**	**50 Marks**
Hours/Week	**4+0+2+0**	**SEE**	**50 Marks**
Total Hours	**52**	**Credits**	**5**

Course Outcomes:

At the end of the course the student should be able to:

1. Introduce the concepts and techniques of design verification
2. Understand the technology challenges and verification technology options.
3. Study different approaches for verification methodologies.
4. Understand the concept of manufacturing tests of digital circuits.
5. Understand fault modeling, simulation, Automatic Test Pattern Generation, BIST etc

UNIT-I

Introduction: VLSI development process, role of testing and verification, verification methodology, Types of Design Verification - Functional Verification, Simulation Emulation.

Block-level Veriifcation. Functional Verification through simulation. Whitebox, blackbox and Graybox testing. Verilog/VHDL test bench for functional verification. **12 Hrs**

UNIT-II

Static Timing Verification. Concept of static timing analysis. Timing constraints, timing models, critical path analysis, false paths.

Physical Design Verification. Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, cross talk. **10 Hrs**

UNIT-III

Fault modeling: defects, errors& fault, Functional Versus Structural Testing, fault models, single stuck at faults

Logic and fault simulation: Modeling circuit for simulatuion, event driven simulation, serial fault simulation **10 Hrs**

UNIT-IV

Testing and verification: how to test chips? VLSI Technology Trends Affecting Testing, test equipments, electrical parametric testing **10 Hrs**

UNIT-V

Test generation & DFT: ATPG for combinational circuit, Design for testability and scan, scan cell design, BIST **10 Hrs**

Reference Books:

R1. M. Bushnell, Vishwani Agrawal, **"Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits",** Kluwer Academic Publishers, 2002.
R2. Prakash Rashinkar, Peter Paterson and Leena Singh **"System – on – a - Chip Verification – Methodology and Techniques"**, Kulwer Academic Publishers, 2001.
R3. Laung-Terng wang, Cheng-Wen wu & Xiaoping Wen, "**VLSI Test Principles and Architectures- Design for Testability",** Morgan Kaufmann,2006.
R4. S. Minato **"Binary Decision Diagram and Applications for VLSI CAD"**, Kulwer Academic Pub. November 1996.
R5. **"An Excellent Source for Instructors for Formal Verification Techniques"** (website developed by) Prof. V. Narayanan, Penn State University, USA. http://www.cse.psu.edu/~vijay/verify/instuctors.html

VLSI DESIGN VERIFICATION-LAB

(USE ANY EDA TOOL)

LIST OF EXPERIMENTS

1. Design and Verification of Ripple Carry Adder

   (Dataflow, Structural, Gate level, Behavioral, Test bench creation)

2. Implement CRC-4 Encoder using HDL Code

   (Dataflow, Structural, Gate level, Behavioral, Test bench creation)

3. Timing Verification of Ripple Carry Adder
4. Gate level analysis of different stuck at faults in a CMOS Gate.(NAND, NOR)
5. Fault analysis for a given logic circuit.
6. Design of a LFSR and calculate the different power dissipation for the circuit (8bit, 16bit, 32 bit) using BIST
7. Perform timing analysis for a given sequential circuit

ELECTIVE-I

MODELING OF DIGITAL SYSTEMS USING VHDL

Course Code	**17VDE111**	**CIE**	**50 Marks**
Hours/Week	**4+0+0+0**	**SEE**	**50 Marks**
Total Hours	**52**	**Credits**	**4**

Course Outcomes:

At the end of the course the student should be able to:

1. Get an insight to the fundamentals of digital logic using Very High Speed Integrated Circuit Hardware Descriptive Language (VHDL).
2. Design networks involving arithmetic operations using VHDL coding.
3. Analyze and design standard combinational modules and Get an insight to the specification, organization and Implementation of RTL systems.
4. Understand data and control subsystems and able to design it.
5. Analyze the specifications and implement a microcomputer system and Learn to design a RTL system for the specifications mentioned .

UNIT-I

INSIDE VHDL: Introduction to VHDL, Specification of combinational systems using VHDL, Basic language element of VHDL, VHDL description of gates, Behavioral Modeling, Data flow modeling, Structural modeling, Subprograms.

10 Hrs

UNIT -II

DESIGN OF NETWORKS FOR ARITHMETIC OPERATIONS: Design of a Serial Adder with Accumulator, State Graph for Control Network, Design of a Binary Multiplier, Multiplication of a Signed Binary Number, and Design of a Binary Divider with VHDL Codes . **08 Hrs**

UNIT-III

STANDARD COMBINATIONAL MODULES: binary decoder, binary encoder, multiplexers and demultiplexers.
REGISTER-TRANSFER LEVEL SYSTEMS: Execution Graph, Organization of System, Implementation of RTL Systems, Analysis of RTL Systems, and Design of RTL Systems. **12 Hrs**

UNIT-IV

DATA AND CONTROL SUBSYSTEM: Data Subsystems, Storage Modules, Functional Modules, Data paths, Control Subsystems, Micro programmed Controller, Structure of a micro programmed controller, Micro instruction Format, Micro instruction sequencing, Micro instruction Timing.

10 Hrs

UNIT-V

SPECIFICATION AND IMPLEMENTATION OF A MICROCOMPUTER: Basic component of a micro system, memory subsystem, I/O subsystem, Processors, Operation of the computer and cycle time.

12 Hrs

Reference Books:

R1. M. Ercegovac, T. Lang and L.J. Moreno, "**Introduction to Digital Systems"**, Wiley,2000
R2. C. H. Roth, **"Digital System Design using VHDL"**, Thomson Learning,2001
R3. J. Bhaskar, **"A VHDL Primer"**, Addison Wesley, 1999
R4. John.F.Wakerly, **"Digital Design-Principles and Practices"**, PHI, 3rd Edition updated, 2005
R5. Douglas Perry, **"VHDL: Programming by Example"**, TMH, 2002
R6. Michae John Sebastian Smith, "**Application-Specific Integrated Circuits"**, Addison-Wesley, 1997

HIGH SPEED VLSI DESIGN

Course Code	**17VDE112**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course Outcomes:

At the end of the course the student will be able to

1. Understand Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures

2. Design Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

3. Know basic Latch design, Latching single-ended logic and Latching Differential Logic.

4. Know Race Free Latch design, Signaling Standards, Chip-to-Chip Communication Networks.

5. Understand timing issues & clock generation.

UNIT-I

Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic **10 Hrs**

UNIT-II

Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise. **12 Hrs**

UNIT-III

Latching Strategies, Basic Latch Design, and Latching single-ended logic, Latching Differential Logic.

10 Hrs

UNIT-IV

Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.

Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection.

10 Hrs

UNIT-V

Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques, Skew Tolerant Design **10 Hrs**

Reference Books:

R1. Kerry Bernstein & et. al., **"High Speed CMOS Design Styles"**, Kluwer, 1999.
R2. Evan Sutherland, Bob stroll, David Harris, **"Logical Efforts, Designing Fast CMOS Circuits",** Kluwer, 1999.
R3. David Harris, **"Skew Tolerant Domino Design"**, Prentice Hall of India Private Ltd, 2000.

SoC DESIGN

Course Code 17VDE113	**CIE Marks 50**
Hrs./ week 4+0+0+0	**SEE Marks 50**
Total Hrs. 52	**Credits 4**

At the end of the course the student should be able to:

1. Understand the benefits and criteria for the design of SoC
2. Understand the architecture, types of processors and memories used in embedded systems.
3. Explain the use of hardware accelerators in a SoC and features of DMA and USB controllers.
4. Explain the different NoC topologies and components in a SoC
5. Explain the SoC design flow

UNIT-I

Motivation for SoC Design - Review of Moore's law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse.

12 Hrs

UNIT-II

Embedded Processors – microprocessors, microcontrollers, DSP and their selection criteria. Review of RISC and CISC instruction sets, Von-Neumann and Harward architectures, and interrupt architectures.

Embedded Memories – scratchpad memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

10 Hrs

UNIT-III

Hardware Accelerators in an SoC – comparison on hardware accelerators and general-purpose CPU. Accelerators for graphics and image processing.

Typical peripherals in an SoC – DMA controller, USB controller. **10 Hrs**

UNIT-IV

Interconnect architectures for SoC-. Bus architecture and its limitations. Network on Chip (NoC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole routing.

Mixed Signal and RF components in an SoC- Sensors, Amplifiers, Data Converters, Power management circuits, RF transmitter and receiver circuits. **10 Hrs**

UNIT-V

SoC Design Flow -IP design, verification and integration, hardware-software codesign, power management problems, and packaging related problems. **10 Hrs**

Reference Books:

R1. Sudeep Pasricha and Nikil Dutt, **"On-Chip Communication Architectures: System on Chip Interconnect"**, Morgan Kaufmann Publishers © 2008

R2. Henry Chang et al., **"Surviving the SOC Revolution: A Guide to Platform-Based Design"**, Kluwer (Springer), 1999 .

R3. Frank Ghenassia, **"Transaction Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems"**, Springer © 2005 (281 pages), ISBN:9780387262321

R4. Luca Benini and Giovanni De Micheli**, "Networks on Chips: Technology and Tools"**, Morgan Kaufmann Publishers © 2006 (408 pages), ISBN:9780123705211

ASIC DESIGN

Course Code 17VDE114	**CIE Marks 50**
Hrs./ week 4+0+0+0	**SEE Marks 50**
Total Hrs. 52	**Credits 4**

Course outcomes:

At the end of the course the student should be able to:

1. Describe the concepts of ASIC design methodology, data path elements, operators, I/O cells.
2. Apply logical effort technique for predicting delay, delay minimization and FPGA architectures.
3. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
4. Explain algorithms for floorplanning and placement of cells for optimized area and speed.
5. Explain and apply routing algorithms for optimization of length and speed.

UNIT-I

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.

CMOS Logic: Datapath Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells. **10 Hrs**

UNIT-II

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages.

Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX. **10 Hrs**

UNIT-III

Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.

Low-level design entry: Schematic entry: Hierarchical design, Netlist screener.

ASIC Construction: Physical Design, CAD Tools.

Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms. **12 Hrs**

UNIT-IV

Floor planning Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.

Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow. **10 Hrs**

UNIT-V

Routing: Global Routing: Goals and objectives, Global Routing Methods, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit extraction and DRC. **10 Hrs**

Reference Books:

R1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison-Wesley Professional, 2005.
R2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
R3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
R4. Rakesh Chadha, Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

ELECTIVE-II

ADVANCED DIGITAL SYSTEM DESIGN

Course Code	**17VDE 121**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course outcomes:

At the end of the course the student should be able to:

1. Define Finite State Model. Design Simplified Synchronous State Machines by evaluating equivalent states.
2. Analyze and Design Asynchronous State Machines Identify the different Hazards and design Hazard free circuits.
3. Define different Fault classes and models Design Fault tests using different techniques.
4. Explain the architecture of RAM, ROM, and FPGAs. Design Digital circuits using Programmable Logic
5. Represent and design Digital Circuits in RTL. Define various elements of ASM Charts and design circuits using ASM

UNIT-I

INTRODUCTION TO SYNCHRONOUS SEQUENTIAL CIRCUITS:Finite State Model- definitions, Synthesis of synchronous sequential Circuits, State Equivalence and Machine Minimization, Simplification of incompletely specified Machines, Iterative networks. **[Reference-1: 9.2-9.4, 9.6, 10.1-10.4]** **12 Hrs**

UNIT-II

ASYNCHRONOUS SEQUENTIAL LOGIC: Introduction, Analysis Procedure, Design Procedure, Reduction of State and Flow Tables, Race Free State Assignment, Hazards, Data synchronizers –Mixed operating mode asynchronous circuits. **[Reference-2: 9.1-9.7, Reference-3: 8.6-8.7]** **12 Hrs**

UNIT-III

FAULT DIAGNOSIS AND TOLERANCE: Fault Classes and Models, Fault table method-path sensitization method – Boolean difference method, The Kohavi Algorithm, Tolerance techniques. **[Reference-4: 6.1-6.9]** **8 Hrs**

UNIT-IV

MEMORY AND PROGRAMMABLE LOGIC: Random Access Memory, Read-only memory, Programmable Logic Array, Programmable Array Logic, Sequential Programmable Devices. **[Reference-2: 7.1-7.8]** **10Hrs**

UNIT-V

ADVANCED DESIGN TECHNIQUES:Register Transfer Level Design- RTL Notations, RTL in Verilog-HDL,Algorithmic State Machines, Design Examples: Sequential Binary Multiplier, Design with Multiplexers. **[Reference-2: 8.1 – 8.10]**

10 Hrs

Reference Books:

R1. ZviKohavi, Niraj K Jha, "**Switching and Finite Automata Theory**" Cambridge University Press, 3rd Edition, 2014

R2. M Morris Mano, Michael Ciletti, "**Digital Design: With an introduction to the Verilog HDL**", Pearson , 5th Edition, 2013

R3. John M Yarbrough, "**Digital Logic: Applications and Design**", Thomson Learning, 2001

R4. Nripendra N Biswas, **"Logic Design Theory"** Prentice Hall of India, 2013

DSP ALGORITHMS & ARCHITECTURE

Course Code	**17VDE122**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course outcomes:

At the end of the course the student should be able to:

1. Choose DSP core for generic DSP applications.
2. Understand transformation and filter structure for the required analysis.
3. Understand array processing in DSP applications
4. Apply DSP algorithm for audio, video and multimedia related system development.
5. Understand different compression techniques in the field of signal processing.

UNIT-I

Introduction to Generic DSP's, Performance and Structural limitations. Measures and Structures for enhancing performance. **12 Hrs**

UNIT-II

Filter structures, Transform structures, Data Flow and Control flow issues. **10 Hrs**

UNIT-III

Introduction to Array processing, Array processing approaches to DSP solutions.

10 Hrs

UNIT-IV

Some modern DSP algorithms (audio, video and multimedia) and development of new computational and arithmetic building blocks. **10 Hrs**

UNIT-V

Architecture development for some Compression and Coding Algorithms. Reference to some standards and development of Architecture based implementation of these. **10 Hrs**

Reference Books:

R1. Keshab K Parhi, **"VLSI Signal Processing Systems"**, John Wiley and Son's, New York, 1999.
R2. Peter Prissch, **"Architectures for Digital Signal Processing"**, Jhon Wiley and Son's, New York, 1998.
R3. Khalid Sayood, **"Introduction in Data Compression"**, 2E Harcourt India, New Delhi, 2000

SOFT COMPUTING

Course Code	**16VDE123**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course Outcomes:

At the end of the course the student should be able to:

1. Answer the situations of real-life such as uncertainty, impression, approximation, partial truth, etc. using nature driven approaches.
2. Develop fuzzy models to solve the wide ranges of uncertainty.
3. Relate and apply global and local optimization methods.
4. Create artificial neural network model in decision support systems.
5. Design computer-aided systems for pattern recognition.

UNIT-I

INTRODUCTION TO SOFT COMPUTING: Evolution of Computing - Soft Computing Constituents – from Conventional Artificial Intelligence to Computational Intelligence, Pattern Recognition and Machine Learning. 1**0Hrs**

UNIT-II

GENETIC ALGORITHMS: Introduction to Genetic Algorithms (GA) –Representation, Evaluation Function, Population, Parent Selection Mechanism, Variation Operators, Survivor Selection Mechanism, Initialization, Termination Condition Mathematical Construction of Genetic Operators, Applications of GA in Machine Learning - Machine Learning Approach to Knowledge Acquisition. **12 Hrs**

UNIT-III

APPLICATIONS OF GENETIC ALGORITHMS: Variants of Binary Encoded Genetic Algorithms: Micro Genetic Algorithm, Messy Genetic Algorithm, Greedy Genetic Algorithm etc. and their usage in Engineering Problems, Real Coded Genetic Algorithms, Differential Evolution and their recent usage in Engineering. **10 Hrs**

UNIT-IV

NEURAL NETWORKS: Introduction to Neural Network, Adaptive Networks – Feed forward Networks, back propagation algorithm, Self Organizing Maps (SOMs). **10 Hrs**

UNIT-V

FUZZY LOGIC: Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions- Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems. Neuro-fuzzy modeling: Fuzzy Expert Systems – Fuzzy Decision Making. **10 Hrs**

Reference Books:

R1. Jyh-Shing Roger Jang, Chuen-Tsai Sun, EijiMizutani, "Neuro-Fuzzy and Soft Computing", PHI, 2003.
R2. De Jong, K. A., "Evolutionary Computation: A Unified Approach", Bradford Books, New York, USA, 2002.
R3. George J. Klir and Bo Yuan, "Fuzzy Sets and Fuzzy Logic-Theory and Applications", PHI, 1995.
R4. James A. Freeman and David M. Skapura, "Neural Networks Algorithms, Applications, and Programming Techniques", Pearson Edn., 2003.
R5. Simon Haykin, "Neural Networks-A Comprehensive Foundation", Prentice-Hall of India, 2nd Edition,2005.
R6. David E. Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning", Addison Wesley, 1997.

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Course Code	**17VDE124**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course Outcomes:

At the end of the course the student should be able to:

1. Explain types of microelectronic designs, levels of abstraction and synthesis process and general approaches to optimization.
2. Analyze graph optimization problems and optimization of graphs, logic minimization using Boolean algebra.
3. Apply HDLs synthesis optimization techniques, HDL compiler optimizations, architectural level synthesis and optimization techniques for data path and control path.
4. Explain and apply logic minimization algorithms and techniques, optimization principles for two level combinational logic.
5. Apply state based model and network based model for sequential circuit optimization, algorithms for area optimal library binding.

UNIT-I

Introduction: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization

Graphs: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications. **10 Hrs**

UNIT-II

Hardware Modeling: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

Schedule Algorithms: A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.

10 Hrs

UNIT-III

Two level combinational logic optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations. **10 Hrs**

UNIT-IV

Multiple level combinational optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization. **10 Hrs**

UNIT-V

Sequential circuit optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Cell library binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding.

12 Hrs

Reference Books:

R1. Giovanni De Micheli, **"Synthesis and Optimization of Digital Circuits",** Tata McGraw-Hill, 2003.

R2. Srinivas Devadas, Abhijit Ghosh, and Kurt Keutzer, **"Logic Synthesis",** McGraw-Hill, USA, 1994.

R3. Neil Weste and K. Eshragian,b, **"Principles of CMOS VLSI Design: A System Perspective",** 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.

R4. Kevin Skahill, **"VHDL for Programmable Logic",** Pearson Education (Asia) Pte. Ltd., 2000.

II – SEMESTER

ADVANCES IN VLSI DESIGN

Course Code	**17VDE201**	**Credits**	**5**
Hours/Week	**4+0+0+1**	**CIE**	**50 Marks**
Total Hours	**52**	**SEE**	**50 Marks**

Course Outcomes:

At the end of the course the student should be able to:

1. Select a suitable semi-custom design approach to design a desired digital system and analyze the MISFET, MOSFET and MODFETs in equilibrium and under bias.
2. Understand the need for super buffers to drive large capacitive loads and analyze the energy band diagrams of MISFETs under different bias.
3. Apprehend the short channel effects and design pass-transistor circuit for given logic.
4. Analyze th effect of scaling, understand the challenges to CMOS technology and revolutionary advances beyond CMOS
5. Design barrel shifter, tally circuit, CMOS multiplexers and apply routing algorithms to determine minimum length path for interconnects.

UNIT- I

Review of MOS Circuits: MOS and CMOS static plots, CMOS switches

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, programmable structure, standard cell approach, Full custom Design, Gate arrays**,** Programmable inter connect **6 Hrs**

MESFET and MODFETs: Structure, operations, quantitative description of MESFETS. **4 Hrs**

UNIT-II

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and small signal analysis of MOSFETS. **4 Hrs**

Super Buffers: NMOS super buffers, NMOS tri-state super buffer and pad drivers, CMOS super buffers, RC delay lines **6 Hrs**

UNIT-III

Short Channel Effects: Two dimensional Potential profile, High electric field in the short channel, Punch-through and channel length modulation. **6 Hrs**

Steering Logic: Driving large capacitive loads, pass-transistor logic, designing pass-transistor logic, Dynamic ratio less inverters, General functional blocks - NMOS and CMOS functional blocks. **5 Hrs**

UNIT -IV

Scaling Theory: Constant filed, constant voltage and quasi-constant voltage models

Beyond CMOS: Evolutionary advances beyond CMOS: SOI MOSFET **4 Hrs**

Revolutionary advances beyond CMOS: carbon Nano-tubes, Conventional vs. tactile computing, molecular and biological computing.

Molectronics-Molecular Diode and diode- diode logic **5 Hrs**

Defect tolerant computing.

Challenges to CMOS: Processing Challenges to Further CMOS Miniaturization.

UNIT-V

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logics, NMOS, CMOS Multiplexers, Barrel shifter. **7 Hrs**

Wire routing Algorithms: Need for algorithms, study of Lee-Moore Maze running algorithm and line search algorithm. **5 Hrs**

Reference Books:

R1. Kevin F Brernnan, **"Introduction to Semiconductor Devices – For Computing and Telecommunications Applications"**, Cambridge University Press, First South Asian Edition,2005

R2. Eugene D Fabricius, **"Introduction to VLSI Design"**, McGraw-Hill International Edition

R3. D.A Pucknell, **"Basic VLSI Design"**, PHI Publication, Third Edition, 2004.

R4. Wayne Wolf, **"Modern VLSI Design"** Pearson Education, Second Edition,2002

ADVANCES IN VLSI DESIGN LAB

(Use any of the EDA Tools)

List of Experiments

1. Design and simulation to implement hierarchy and regularity in a design: Develop Verilog code and perform simulation using testbench for:

   . Adder

   . Transmission Gate based multiplexer

   . Synchronous and asynchronous counters

2. Design and simulation Pass-Transistor logic (PT logic) for various logic functions.

3. Schematic simulation of a given logic function using:

   . NAND-NAND logic

   . NOR-NOR logic

   . AOI logic

4. Design and simulation of a talley circuit.

5. Design and simulation of a barrel shifter.

DESIGN OF ANALOG VLSI CIRCUITS

Course Code	**17VDE202**	**CIE Marks**	**50**
Hrs./Week	**4+0+2+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**5**

Course Outcomes:

At the end of the course the student should be able to:

1. Explain MOSFET operation, characteristics, second order effects and device models
2. Design and analyze single stage amplifiers using MOSFETs.
3. Design and analyze differential amplifiers using MOSFETs and current mirrors.
4. Analyze the high frequency behavior and noise in analog circuits using MOSFETs
5. Design and analyze operational amplifiers using MOSFETs, Implement oscillators, VCO and PLL in CMOS technology.

UNIT-I

Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models. MOS Device as a Capacitor **8 Hrs**

UNIT-II

Single stage Amplifier: CS stage with resistance load, diode connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascode stage, Folded cascode, choice of device models. **10 Hrs**

UNIT-III

Differential Amplifiers: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell.

Passive and active Current mirrors: Basic current mirrors, Cascode current mirrors, active current mirrors. **12 Hrs**

UNIT-IV

Frequency response of Amplifier: General considerations, Common source stage**,** source follower, Common gate stage, Cascode stage and Difference pair. Noise in CS stage, CG stage, source follower, cascode stage, differential pair. **12 Hrs**

UNIT-V

Operational Amplifiers: One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compenastion of two stage OP-Amp, Other compensation techniques.

Oscillators: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO.

PLL: Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. **10 Hrs**

Reference Books:

R1. Behzad Razavi, **"Design of Analog CMOS Integrated Circuits",** TMH, 2007.
R2. R. Jacob Baker, Harry W. Li., David E. Boyce, **"CMOS : Circuit Design , Layout and Simulation ",** PHI, 2003

ANALOG & MIXED MODE VLSI LAB

LAB EXPERIMENTS:

Tool to be used: CADANCE/SYNOPSIS/MENTOR GRAPHICS.

1. Design a single stage amplifier using MOSFETs for the given specifications.
2. Design a differential amplifier using MOSFETs for the given specifications.
3. Design a two stage op-amp for the given specification. Determine the frequency response, slew rate, offset effects and Noise.
4. Design a simple sample and hold circuit and measure the switching times.

Design flow:

1. Draw the schematic and verify the following
2. DC Analysis
3. AC Analysis
4. Transient Analysis
5. Draw the Layout and verify the DRC, ERC
6. Check for LVS

REAL TIME OPERATING SYSTEMS

Course Code	**17VDE203**	**CIE Marks**	**50**
Hrs./Week	**4+0+2+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**5**

Course Outcomes:

After studying this subject, the student should be able to:

1. Know the history of real-time operating systems, and acquire knowledge on basic concepts of RTOS such as utility, scheduling and its theories, RTOS characteristics etc.
2. Examine the operational principle of different scheduling algorithms and their characteristics.
3. Analyze concepts related to I/O and Memory resources, examine basic problems faced by multi-resource services, and solve challenges faced by soft real time services.
4. Recognize and resolve software and hardware challenges faced by real-time system to meet service deadlines, and get awareness on embedded system components and debugging components.
5. Analyze basic performance tuning procedures to design better systems, and explore high reliability and high availability designs.

Unit-I

Introduction to Real-Time Embedded Systems: Brief History if Real-Time Systems, a Brief History of Embedded Systems.

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS and its characteristics, Thread Safe Reentrant Functions. **12 Hrs**

Unit-II

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic Least Upper Bound, Necessary and Sufficient Feasibility, Deadline – Monotonic Policy, Dynamic Priority Policies, EDF Algorithm, Multiprocessor Scheduling Algorithms. **10 Hrs**

Unit-III

I/O Resources: Worst-Case Execution Time, Intermediate I/O, Execution Efficiency, I/O Architecture.

Memory: Physical Hierarchy, Capacity and Allocation, Shared Memory, ECC Memory: Illustration using Hamming encoding, Flash Fill Systems.

Multi-Resource Services: Blocking, Deadlock and Livestock, Critical sections to Protect Shared Resources, Priority Inversion and its solutions.

Soft-Real-Time Services: Missed Deadlines, Quality of Service, Alternatives to Rate Monotonic Policy, Mixed Hard and Soft Real-Time Services. **10 Hrs**

Unit-IV

Embedded System Components: Firmware Components, RTOS System Software Mechanisms, Software Application Components.

Debugging Components: Exceptions, Asserts, Checking Return Codes, Single-Step Debugging, Test Access Ports, Trace Ports, Power-On Self-Test and Diagnostics, Application Level Debugging.

10 Hrs

Unit-V

Performance Tuning: Basic Concepts of Drill-Down Tuning, Hardware-Supported Profiling and Tracing, Building Performance Monitoring into Software, Path Length, Efficiency, and Call Frequency, Fundamental Optimizations.

High Availability and Reliability Design: Reliability and Availability, Similarities and Differences, Reliability, Reliable Software, Available Software, Design Trade Offs, Hierarchical Applications for Fail-Safe Design.

Design of RTOS: PIC Microcontroller.

Case Studies Based on MUCOS, VxWorks such as ACVM, Sending Application Layer Byte Streams on TCP/IP Stack, and Smart Card Application. **10 Hrs**

Reference Books:

R1. Sam Siewert, "**Real-Time Embedded Systems and Components**", Cengage Learning India Edition, 2007.

R2. Raj Kamal, "**Embedded System- Architecture, programming and Design**", 2nd Edition, Tata McGraw-Hill Education Pvt. Ltd., 2008

R3. Myke Predko, "**Programming and Customizing the PIC Microcontroller**", 3rd Edition, TMH, 2008.

R4. C.M. Krishna, Kang G Shin, "**Real Time Systems**", McGraw-Hill, 1997.

R5. Dreamtech Software Team, "**Programming for Embedded Systems**", John Wiley, India Pvt. Ltd., 2008.

Real Time Operating Systems LAB

Program List

Use RT-LINUX/SOLARIS/QNX Operating System ONLY.

1. Write a program for Thread Creation and Termination.
2. Create independent threads each of which will execute some function and wait till threads are complete before main continues. Unless we wait run the risk of executing an exit which will terminate the process and all threads before the threads have completed.
3. Create the N number of threads and find the how many threads are executed.
4. Create threads numbers 1-3 and 8-10 as permitted by functionCount1 and create threads number 4-7 as permitted by functionCount2 and print final count value.
5. Design and execute a program using any thread library to create the number of thread specified by the user, each thread independently generates a random integer as an upper limit and then computes and prints the number of primes less than or equal to that upper limit, along with that upper limit.
6. Rewrite above program (Program 5) such that the processes instead of thread are created and the number of child processes created is fixed as two. The program should make use of kernel timer to measure and print the real time, processor time, User space time and kernel space time for each process.
7. Design develop and implement a process with a producer thread and a consumer thread which make use of a bounded buffer (Size can be prefixed at suitable value) for communication. Use any suitable synchronization construct.
8. Design develop and execute a program to solve a system of n liner equations using successive over-relaxation method and n processes which use shared memory API.

ELECTIVE-III

ADVANCED COMPUTER ARCHITECTURE

Course Code	**17VDE211**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**5**

Course Outcomes:

At the end of the course the student should be able to:

1. Analyze the fundamental issues in architecture design and their impact on application performance.
2. Understand advanced issues in design of computer processors, caches, and memory.
3. Analyze performance trade-offs in computer design.
4. Apply knowledge of processor design to improve performance in algorithms and software systems.
5. Acquire experience with tools for statistical analysis of instruction set trade-offs.

UNIT – I

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multifactor and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.

10 Hrs

UNIT – II

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

10 Hrs

UNIT – III

Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors.

10 HRS

UNIT – IV

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

10 Hrs

UNIT - V

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, and MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, and synchronization. Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.
Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine checks, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.

12 Hrs

REFERENCE BOOKS:

R1. Kai Hwang, **"Advanced Computer Architecture"**, TMH.
R2. Hwan and Briggs, **" Computer Architecture and Parallel Processing"**, MGH.VLSI
R3. D. A. Patterson and J. L. Hennessey, **"Computer organization and Design"**, Morgan Kaufmann, 2nd Ed.
R4. Kai Hwang and Zu, **"Scalable Parallel Computers Architecture",** MGH.
R5. M.J Flynn, **"Computer Architecture, Pipelined and Parallel Processor Design"**, Narosa Publishing.
R5. D.A.Patterson, J.L.Hennessy, **"Computer Architecture: A quantitative approach"**, Morgan Kauffmann, 2002.

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ALGORITHMS FOR VLSI

Course Code	**17VDE212**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Mark**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course outcomes:

At the end of the course the student should be able to:

1. Explain and apply graph minimization algorithms.
2. Write code for algorithms used for computational and geometrical simplification and minimization using data structures for CAD tools.
3. Explain and write code for partitioning, floorplanning, chip planning and pin assignment.
4. Explain different algorithms used for placement of cells during the physical design of a chip.
5. Explain and write code for algorithms used for routing of cells, clock and power supply.

UNIT-I

Graph Algorithms: Graph search Algorithms, Spanning tree Algorithm, Shortest path Algorithm, Matching Algorithm, Min cut and Max cut Algorithms and Steiner Tree Algorithm. **10 Hrs**

UNIT-II

Computational geometry Algorithms: Line sweep method and extended line sweep method.

Basic data structures: Linked list of blocks, Bin based method, neighbor pointers and corner stitching.

Graph Algorithms for physical design: Classes of graphs in physical design, relationship between graph classes, graph problems, Algorithms for interval graphs and Algorithms for permutations graphs.

10 Hrs

UNIT-III

Partitioning: Group migration Algorithms.
Floor planning and Pin assignment: floor planning, chip planning and pin assignment. **10 Hrs**

UNIT-IV

Placement: Simulated annealing, simulated evolutions, force directed placement, sequence pair technique, Breuer's Algorithm, Terminal propagation Algorithm, Cluster growth and quadratic assignment.

10 Hrs

UNIT-V

Routing: Maze routing Algorithms: Lee's Algorithm, Soukup's Algorithm and Hadlock's Algorithm. Shortest path algorithm, Steiner tree based Algorithm. Single layer routing Algorithms and two layer routing Algorithms.

Over the cell routing, Via minimization, clock, power and ground routing. **12 Hrs**

Reference books:

R1. Naveed Sherwani, **"Algorithms for VLSI Physical Design Automation"** 3rd edition, Springer international, 1998.

R2. Pinaki Mazumber, Elizabeth M Rudnick, "**Genetic Algorithms For VLSI Design, Layout & Test Automation"**, Pearson education,2007.

LOW POWER VLSI DESIGN

Course Code	**17VDE213**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course outcomes:

At the end of the course the student should be able to:

1. Analyze the different types of power dissipation in VLSI Circuits
2. Understand the different techniques of power estimation and analysis
3. Understand the different approaches of Low power design at circuit level
4. Understanding the different low power architecture and systems
5. Understand the different approaches of low power clock distribution and algorithm and architectural level methodologies

UNIT-I

Introduction : Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

12 Hrs

UNIT-II

Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Data Correlation Analysis in DSP Systems, Monte Carlo simulation.

Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

10 Hrs

UNIT-III

Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

10 Hrs

UNIT-IV

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

10Hrs

UNIT-V

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.

Algorithm and Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis and optimization, Architectural level estimation & synthesis.

10 Hrs

Reference Books:

R1. Kaushik Roy, Sharat Prasad, "**Low-Power CMOS VLSI Circuit Design**", Wiley, 2000
R2. Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", KAP, 2002
R3. Rabaey, Pedram, "**Low Power Design Methodologies**", Kluwer Academic, 1997
R4. Anantha P. Chandrakasan & Robert W. Brodersen, **"Low Power Digital CMOS Design"** Kluwer Academic Publications, 1994.

NANOTECHNOLOGY

Course Code	**17VDE214**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course outcomes:

At the end of the course the student should be able to:

1. Understand the broad overview of Nano technology, material, manufacturing and applications in the field of renewable energy.
2. Understand the growth of zero dimensional nano-structures
3. Understand the growth of one dimensional nano-structures
4. Understand the growth of two dimensional nano-structures
5. Understand the thin film fundamentals and transport phenomena

Unit-I

Introduction Overview of nano-technolgy

Materials and manufacture Nanoengineering of polymer bio-medical devices, nano-powder production, nanomaterial technology, nanotechnology devices, nanoparticles manufacture, analytical methods for nanotechnology.

Nanotechnology for renewable energy Energy intensity of materials, hydrogen energy, battery technology, nanotechnology alternative to existing batteries, fuel cell technology, power generation using nanotechnology, solar energy and nano technology, wind power and nanotechnology. **12 Hrs**

Unit- II

ZERO DIMENSIONAL NANO-STRUCTURES Nano particles through homogenous nucleation; Growth of nuclei, synthesis of metallic nano particles, Nano particles through heterogeneous nucleation; Fundamentals of heterogeneous nucleation and synthesis of nano particles using micro emulsions and Aerosol.

10 Hrs

Unit-III

One Dimensional Nano-structure, Nano-wires and Nano-rods Spontaneous growth: Evaporation and condensation growth, vapor-liquid-solid growth, stress induced recrystallization. Template based synthesis: Electrochemical deposition, Electrophoretic deposition. Electro spinning and Lithography. **10 Hrs**

Unit-IV

Two Dimensional nano-structures: Fundamentals of film growth. Physical vapour Depostion (PVD): Evaporation molecular beam epitaxy (MBE), Sputtering, Comparison of Evaporation and sputtering. Chemical Vapour Depostion (CVD) : Typical chemical reactions, Reaction kinetics, transport phenomena, CVD methods, diamond films by CVD. **10 Hrs**

Unit-V

Thin Films Atomic layer deposition (ALD), Electrochemical deposition (ECD), Sol-Gel films, Advantages, Disadvantages and Applications of thin films

Transport Phenomena Confinement and Transport in nanostructure, Current, Reservoirs and Electron channels, Conductance formula for nanostructures, Quantized conductance. Local density of states. Ballistic transport, Coulomb blockade, Diffusive transport. **10 Hrs**

References:

R1. Nano structures and Nano materials: Synthesis, properties and applications by Guozhong Cao, Imperial College press, 2004.
R2. Nanotechnology – Importance and Applications, M H Fulekar, New Age International limited, 2nd edition,2010
R3. Quantum wells, Wires & Dots,: Theoretical & Computational Physics of Semiconductors Nanostuructures, Paul Harrison, Alex Valavanis, 4th edition, 2016.
R4. Handbook of nanotechnology, Bhusha, Springer 2004
R5. Nano optoelectronics, M.Grundman, Springer 2002.
R6. Nanophotonics , Paras N.Prasad, Wiley Blackwell, 2004.

ELECTIVE-IV

SYSTEM DESIGN USING EMBEDDED PROCESSORS

Course Code	**17VDE221**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course Outcomes:

At the end of the course the student should be able to:

1. Learn the architecture, instruction set and program the 8051 microcontroller.
2. Understand the architecture, programming model and memory organization of 32- bit ARM920T processor.
3. Learn ARM, Thumb instruction set and the interrupt handling of ARM920T processor.
4. Understand the architecture and peripherals of ARM9 microcontroller.
5. Be familiar with development & debugging tools for microcontroller based embedded systems.

UNIT-I

8-Bit Microcontrollers:
Architecture: CPU Block diagram, Memory Organization, Program memory, Data Memory, Interrupts
Peripherals: Timers, Serial Port, I/O Port
Programming: Addressing Modes, Instruction Set, Programming
Microcontroller based System Design: A typical application design from requirement analysis through concept design, detailed hardware and software design using 8-bit 8051 Microcontrollers.

12 Hrs

UNIT-II

32- Bit ARM920T Processor Core:
Introduction: RISC/ARM Design Philosophy, About the ARM920T Core, Processor Functional Block Diagram
Programmers Model: Data Types, Processor modes, Registers, General Purpose Registers, Program Status Register, CP15 Coprocessor, Memory and memory mapped I/O, Pipeline, Exceptions, Interrupts and Vector table, Architecture revisions, ARM Processor Families.
Memory Management Units: How virtual memory works, Details of the ARM MMU, Page Tables, Translation Look-aside Buffer Domains and Memory access permissions **10 Hrs**

UNIT-III

ARM Instruction Set: Data Processing instructions, Branch instructions, Load - Store instructions, Software Interrupt Instruction, Program Status Register Instruction, Loading Constants
Thumb Instruction Set: Thumb register usage, ARM-Thumb interworking, Branch instruction,

Data processing instructions, Load - store instructions, stack instructions, software interrupt instructions.
Interrupt Handling: Interrupts, Assigning interrupts, Interrupt latency, IRQ & FIQ exceptions, Basic interrupt stack design, and implementation, Non-nested Interrupt handler. **10 Hrs**

UNIT-IV

ARM9 Microcontroller Architecture:
AT91RM9200 Architecture: Block Diagram, Features, Memory Mapping
Memory Controller (MC): Memory Controller Block Diagram, Address Decoder, External Memory Areas, Internal Memory Mapping.
Parallel Input/output Controller (PIO).
Interrupt Controller: Normal Interrupt, Fast Interrupt, AIC.
System Timer (ST): Period Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT),Real Time Clock (RTC)

10 Hrs

UNIT-V

Development & Debugging Tools for Microcontroller based Embedded Systems:
Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc. **10 Hrs**

Reference Books:

R1. Andrew N Sloss, Dominic Symes, Chris Wright, **"ARM System Developer's Guide - Designing and Optimizing System Software"**, Elsevier, 2006
R2. Ayala, Kenneth J, **"8051 Microcontroller - Architecture, Programming & Applications"**, 1st edition, Penram International Publishing, 1991.
R3. Raj Kamal, **"Microcontroller - Architecture Programming Interfacing and System Design"**, 1st Edition, Pearson Publication,2005.
R4. Joseph Yiu, **"The Definitive Guide to the ARM Cortex-M3",** Newnes,(Elsevier), 2008.

MEMS AND IC INTEGRATION

Course Code	**17VDE222**	**CIE Marks**	**50**
Hrs./Week	**4+0+0+0**	**SEE Marks**	**50**
Total Hrs.	**52**	**Credits**	**4**

Course Outcomes:

At the end of the course the student should be able to:

1. Understand CMOS IC Fabrication
2. Understand the MEMS Design methodology
3. Understand various Mechanical Sensors and its applications
4. Understand various Electronics Sensors and its applications
5. Understand the scaling issues in MEMS

UNIT-I

Overview of CMOS process in IC fabrication – Crystal growth, doping, Growth and deposition of dielectric layers, epitaxial growth, masking and photolithography, etching, metallization, surface and bulk micromachining, LIGA process, wafer bonding. **12 Hrs**

UNIT-II

MEMS system-level design methodology, Equivalent Circuit representation of MEMS, signal-conditioning circuits, and sensor noise calculation. **10 Hrs**

UNIT-III

Pressure sensors with embedded electronics (Analog/Mixed signal), Accelerometer with transducer, Gyroscope, Bolo meter **10 Hrs**

UNIT-IV

RF MEMS, Optical MEMS

10 Hrs

UNIT-V

MEMS scaling issues **10 Hrs**

Reference Books:

R1. Gandhi S.K., **"VLSI Fabrication principles"**, John Wiley and sons, 1983
R2. Gregory T.A. Kovacs, **"Micromachined Transducers Sourecbook"**, The McGraw-Hill, Inc. 1998
R3. Stephen D. Senturia, **"Microsystem Design",** Kluar Publishers, 2001
R4. Nadim Maluf, **"An Introduction to Microelectromechanical Systems Engineering"**, Artech House, 2000.
R5. M.H. Bao, **"Micro Mechanical Transducers",** Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000.
R6. Masood Tabib-Azar, **"Micro actuators"**, Kluwer, 1998.

R7. Ljubisa Ristic, Editor, **"Sensor Technology and Devices",** Artech House, 1994.
R8. D. S. Ballantine, et. al., **"Acoustic Wave Sensors",** Academic Press, 1997.
R9. H. J. De Los Santos, **"Introduction to Micro electro- mechanical (MEM) Microwave Systems"**, Artech, 1999.
R10. James M.Gere and Stephen P. Timoshenko, **"Mechanics of Materials",** 2nd Edition, Brooks/Cole Engineering Division, 1984.

VLSI SIGNAL PROCESSING

Course Code 17VDE223	**CIE Marks 50**
Hrs./ week 4+0+0+0	**SEE Marks 50**
Total Hrs. 52	**Credits 4**

Course Outcomes:

At the end of the course the student will be able to

1. Explain pipelining, parallel processing & data flow representation.
2. Understand retiming, unfolding, algorithmic strength reduction in filters
3. Know fast convolution, systolic architecture.
4. Understand digital lattice filter structures, bit level arithmetic architecture.
5. Know low power design, programmable digital signal processors & their applications.

UNIT-I

Introduction to DSP systems – Data flow representations - Iteration Bound – Pipelined and parallel processing. **12 Hrs**

UNIT-II

Retiming – unfolding – algorithmic strength reduction in filters and transforms. **10 Hrs**

UNIT-III

Systolic architecture design – fast convolution – pipelined and parallel recursive and adaptive filters. **10 Hrs**

UNIT-IV

Scaling and round off noise – digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic. **10 Hrs**

UNIT-V

Numerical strength reduction – synchronous, wave and asynchronous pipelines – low power design – programmable digit signal processors & applications. **10 Hrs**

Reference Books:

R1. Keshab K. Parthi, **"VLSI Digital signal processing systems, Design and Implementation"**, Wiley, Inter Science, 1999.
R2. Mohammad Ismail, Terri Fiez, **"Analog VLSI: Signal and Information Processing",** McGraw Hill, 1994
R3. S.Y. Kung, H.J. White House, T. Kailath, **"VLSI and Modern Signal Processing"**, Prentice Hall, 1985.

CMOS RF CIRCUIT DESIGN

Course Code 17VDE224	**CIE Marks 50**
Hrs./ week 4+0+0+0	**SEE Marks 50**
Total Hrs. 52	**Credits 4**

Course Outcomes:

At the end of the course the student should be able to:

1. Understand the basic concepts of RF design and behavior of passive components
2. Realize the behavior of BJT and MOSFET parameters at RF range
3. Apply the Smith chart and design high frequency amplifiers
4. Explain the biasing and referencing in devices at RF range and identify different kinds of noise
5. Design RF circuits and explain RF synthesizers.

UNIT-I

Introduction to RF design and Wireless Technology:

Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion, characteristics of passive IC components, resistor, capacitor and inductor.

10 Hrs

UNIT-II

BJT and MOSFET Behavior at RF Frequencies:

BJT and MOSFET Behavior at radio frequencies, Modeling of the Transistors, Noise Performance and Limitations of Devices, Integrated Parasitic Elements at High Frequencies and their Monolithic Implementation.

10 Hrs

UNIT-III

The Smith chart: S – parameters.

High-frequency Amplifier Design: Zeros as bandwidth enhancers, Shunt-series amplifier, Bandwidth enhancement with f_T doublers, Tuned amplifiers, Neutralization and unilateralization, Cascaded amplifiers.

10 Hrs

UNIT-IV

Voltage Reference and Biasing:

Review of diode behavior, Diodes and Bipolar Transistors in CMOS technology, Supply-independent bias circuits, Band gap voltage reference, Constant-gm bias.

Noise: Thermal noise, Short noise, Flicker noise, Popcorn noise, Classical two-port noise theory, Examples of noise calculations.

10 Hrs

UNIT-V

RF Circuits Design:

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, various mixers-working and implementation.

Oscillators -Basic topologies VCO and definition of phase noise, Noise power and trade off.

Radio frequency Synthesizers - PLLS, Various RF synthesizer architectures and frequency dividers,

Design issues in integrated RF filters.

12 Hrs

Reference Books:

R1. Thomas H. Lee, "Design of CMOS RF Integrated Circuits", Cambridge University press, 1998.
R2. B. Razavi, "RF Microelectronics", PHI Learning, 1998.
R3. R. Jacob Baker, H.W. Li, D.E. Boyce, "CMOS Circuit Design, Layout and Simulation", PHI Learning, 1998.
R4. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology", TMH, 1996.

LabVIEW Basics

Course Code AP006	**CIE Marks 50**
Hrs./ week 2+0+0+0	**SEE Marks 50**
Total Hrs. 26	**Credits Nil**

Syllabus:

1. Introduction to LabVIEW: Front panel, Block diagram, Tool palette, Control palette, Run, stop, and abort.
2. Numerical palette, String palette, Boolean palette and Comparison palette.
3. Case structure, formula structure.
4. Manipulating Arrays: Build, Search, Concatenate and Sub arrays.
5. The while loop and its applications: Need for time delay; Different ways of connecting the conditional terminal.
6. For Loop: applications and examples to fill array.
7. Use of shift registers for using data from previous iterations, applications.
8. Manipulating strings with examples.
9. Clusters: Combining multiple data types to form clusters. Error cluster and its significance, and their use.
10. Graphs and charts, creating 3D graphs.
11. Project work.

Evaluation based on Hands-On tasks during the course.