Syllabus and Scheme of Examination

M.Tech. in VLSI DESIGN AND EMBEDDED SYSTEMS

2017-18

Institution
Vision - Pursuing Excellence, Empowering people, Partnering in Community Development.

Mission - To develop NMAM Institute of Technology, Nitte, as Center of Excellence by imparting Quality Education to generate Competent, Skilled and Humane Manpower to face emerging Scientific, Technological, Managerial and Social Challenges with Credibility, Integrity, Ethics and Social Concern.

Department:

Vision Statement:
Empowering people, Partnering in community development and achieving expertise in the field of Electronics and Communication.

Mission Statement:
To impart effective knowledge of state of the art technology in the field of Electronics and Communication that contributes to the socio-economic development and to generate technical manpower with high degree of credibility, integrity and ethical standards by providing vibrant learning environment.

Programme Educational Objectives
**PEO1:** Pursue successful careers in industry, academia and entrepreneurial ventures in the domain of VLSI Design and Embedded Systems.

**PEO2:** Identify & apply appropriate Electronic Design Automation (EDA) to solve real time / research problems in VLSI & Embedded Systems domain.

**PEO3:** Engage in development activity and add value to the socio-economic development of the region.

**Programme Outcomes**

**PO1:** An ability to independently carry out research / investigation and development work to solve practical problems

**PO2:** An ability to write and present a substantial technical report / document

**PO3:** Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

**PO4:** An ability to function, manage and lead multidisciplinary teams.
# Scheme of Teaching and Examination for M. Tech. VLSI Design and Embedded Systems

Revised at the BOS meeting on 19-05-2017

## I Semester

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Name of the Course</th>
<th>Contact hours/week</th>
<th>Duration of Sem. End Exams in hours</th>
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<tbody>
<tr>
<td>17VDE101</td>
<td>Embedded System Design</td>
<td>4/0/2/0</td>
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<td>17VDE102</td>
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<tr>
<td>17VDE103</td>
<td>VLSI Design Verification</td>
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<td>Research Experience through Practice - I</td>
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<tr>
<td>17VDE111</td>
<td>Modeling of Digital Systems using VHDL</td>
<td>5</td>
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<tr>
<td>17VDE121</td>
<td>Advanced Digital System Design</td>
<td>5</td>
</tr>
<tr>
<td>17VDE112</td>
<td>High Speeds VLSI Design</td>
<td>5</td>
</tr>
<tr>
<td>17VDE122</td>
<td>DSP Algorithms &amp; Architecture</td>
<td>5</td>
</tr>
<tr>
<td>17VDE113</td>
<td>SoC Design</td>
<td>5</td>
</tr>
<tr>
<td>17VDE123</td>
<td>Soft Computing</td>
<td>5</td>
</tr>
<tr>
<td>17VDE114</td>
<td>ASIC Design</td>
<td>5</td>
</tr>
<tr>
<td>17VDE124</td>
<td>Synthesis and optimization of Digital Circuits</td>
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**TOTAL** 15 350 250 25

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<td>Advanced Digital System Design</td>
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<td>High Speeds VLSI Design</td>
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<tr>
<td>17VDE122</td>
<td>DSP Algorithms &amp; Architecture</td>
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<td>17VDE113</td>
<td>SoC Design</td>
<td>5</td>
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<td>17VDE123</td>
<td>Soft Computing</td>
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<tr>
<td>17VDE114</td>
<td>ASIC Design</td>
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**M.TECH. VLSI DESIGN AND EMBEDDED SYSTEMS (AUTONOMOUS SCHEME)**
## II SEMESTER

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Name of the Course</th>
<th>Teaching hours/week</th>
<th>Duration of Exam in hours</th>
<th>Marks for CIE</th>
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<tbody>
<tr>
<td>17VDE 201</td>
<td>Advances in VLSI Design</td>
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<td>Design of Analog VLSI Circuits</td>
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<td>Real Time Operating Systems</td>
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### ELECTIVE – III

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<tbody>
<tr>
<td>17VDE211</td>
<td>Advanced Computer Architecture</td>
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<tr>
<td>17VDE212</td>
<td>Algorithms for VLSI</td>
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<tr>
<td>17VDE213</td>
<td>Low Power VLSI Design</td>
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<tr>
<td>17VDE214</td>
<td>Nanotechnology</td>
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### ELECTIVE – IV

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<tbody>
<tr>
<td>17VDE221</td>
<td>System Design Using Embedded Processors</td>
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<tr>
<td>17VDE222</td>
<td>MEMS and IC Integration</td>
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<tr>
<td>17VDE223</td>
<td>VLSI Signal Processing</td>
</tr>
<tr>
<td>17VDE224</td>
<td>CMOS RF Circuit Design</td>
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</tbody>
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List of Audit courses currently offered:

- LabVIEW Basics
M.TECH. VLSI ESIGN AND EMBEDDED SYSTEMS  
(AUTONOMOUS SCHEME)

III SEMESTER

Revised at the BOS meeting on 19-05-2017

<table>
<thead>
<tr>
<th>Course Code</th>
<th>Name of the Course</th>
<th>Duration</th>
<th>Marks for Practical/Field Work/Assignment</th>
<th>Total Credits</th>
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<tr>
<td>17VDE 301</td>
<td>Industrial Training Mini-Project</td>
<td>Full time 8 weeks</td>
<td>50 (report) 50 (presentation)</td>
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<tr>
<td>17VDE 302</td>
<td>Seminar on special topics</td>
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<tr>
<td>17VDE303</td>
<td>Project-Part I</td>
<td>Full time 10 weeks</td>
<td>100 (report) 100 (presentation)</td>
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IV SEMESTER

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<thead>
<tr>
<th>Course Code</th>
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<th>Duration</th>
<th>Duration of Exam in Hrs.</th>
<th>Marks for</th>
<th>Total Credits</th>
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| 17VDE 401   | Project -Part II   | Full time 20 weeks | 200 [PPE’-I – 100  

PPE-II – 100] | 200 | 30             |
| TOTAL       |                     |           |                           | 400       | 30            |

GRAND TOTAL From 1st to 4th semester: 100 credits (2000 marks)

PPE* – Project Progress Evaluation
I - SEMESTER

EMBEDDED SYSTEM DESIGN

Course Code: 17VDE101
Credits: 5
Hours/Week: 4+0+2+0
Total Hours: 52

Course Outcomes:

At the end of the course the student should be able to:

1. Get an insight to the fundamentals and know the general structure of an Embedded System.
2. Understand the Hardware/Software Co-Design involved in an Embedded System.
3. Identify problems and design challenges involved in an Embedded System and program using Embedded C.
4. Understand how RTOS is involved in Embedded System Design.
5. Learn IDE and understand the new trends in embedded industry.

UNIT-I

8 Hrs

UNIT-II
Characteristics and Quality Attributes with Introduction to Hardware software Co-Design:

10 Hrs

UNIT-III

12 Hrs

UNIT-IV
Real-Time Operating System (RTOS) based Embedded System Design:
Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling; Putting them altogether, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS.

12 Hrs
UNIT-V

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target Hardware Debugging, Boundary Scan.


10 Hrs

Reference Books:


LIST OF EXPERIMENTS FOR EMBEDDED SYSTEM DESIGN LAB:

1. Write a C code to interface input device (Keyboard), with output devices (seven segment LED’s and free running LEDs) and display the contents of the key pressed on the output.

2. Design a low pass FIR Filter using simulink blocksets.

2. Verilog/VHDL File Processing (Reading a file and storing data in a file).

3. Verilog/ VHDL LCD Display (Scrolling blinking etc.).
CMOS VLSI DESIGN

Course Code          17VDE102                  Credits          5
Hours/Week           4+0+2+0                   CIE               50 Marks
Total Hours          52                        SEE               50 Marks

Course Outcomes:

At the end of the course the student should be able to:

1. Explain MOSFET structure, I-V characteristics, drain current equation and second order effects.
2. Explain CMOS process technology, technology scaling, physical design of CMOS circuits.
3. Design MOS Combinational and sequential circuits
4. Design dynamic logic circuits, design CMOS circuits for driving large capacitive load.
5. Explain clocking in CMOS circuits.

UNIT-I
MOS Transistor Theory: n MOS / p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. Mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, tristate inverter, BiCMOS inverter.

UNIT-II
CMOS Process Technology: Semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD, refractory gate, multilayer inter connect) , Circuit elements, resistor, capacitor, interconnects, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

UNIT-III
UNIT-IV

Dynamic Logic Circuits – Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuits techniques, Dynamic CMOS circuit techniques
Sheet resistance & standard unit capacitance concepts, delay unit time, inverter delays, driving capacitive loads, propagate delays.

UNIT-V

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS., Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements.

Reference Books:


CMOS VLSI DESIGN LAB

(Use any of the EDA Tools)

List of Experiments

1. V-I characteristics of NMOSFET
2. Schematic simulation of CMOS Inverter, analysis of the effect of MOSFET sizing on the inverter midpoint voltage.
3. Layout simulation for a CMOS inverter
4. Schematic simulation of area efficient full adder
5. Schematic simulation of transmission gate
6. Schematic simulation of D flip-flop
7. Schematic simulation domino CMOS circuits
VLSI DESIGN VERIFICATION

Course Code  17VDE103
Hours/Week  4+0+2+0
Total Hours  52

CIE  50 Marks
SEE  50 Marks
Credits  5

Course Outcomes:

At the end of the course the student should be able to:

1. Introduce the concepts and techniques of design verification
2. Understand the technology challenges and verification technology options.
3. Study different approaches for verification methodologies.
4. Understand the concept of manufacturing tests of digital circuits.
5. Understand fault modeling, simulation, Automatic Test Pattern Generation, BIST etc

UNIT-I
Introduction: VLSI development process, role of testing and verification, verification methodology, Types of Design Verification - Functional Verification, Simulation Emulation.

Block-level Verification. Functional Verification through simulation. Whitebox, blackbox and Graybox testing. Verilog/VHDL test bench for functional verification. 12 Hrs

UNIT-II
Static Timing Verification. Concept of static timing analysis. Timing constraints, timing models, critical path analysis, false paths.
Physical Design Verification. Layout rule checks and electrical rule checks. Parasitic extraction. Antenna, cross talk. 10 Hrs

UNIT-III
Fault modeling: defects, errors & fault, Functional Versus Structural Testing, fault models, single stuck at faults
Logic and fault simulation: Modeling circuit for simulation, event driven simulation, serial fault simulation 10 Hrs

UNIT-IV
Testing and verification: how to test chips? VLSI Technology Trends Affecting Testing, test equipments, electrical parametric testing 10 Hrs

UNIT-V
Test generation & DFT: ATPG for combinational circuit, Design for testability and scan, scan cell design, BIST 10 Hrs
Reference Books:

R5. “An Excellent Source for Instructors for Formal Verification Techniques” (website developed by) Prof. V. Narayanan, Penn State University, USA. http://www.cse.psu.edu/~vijay/verify/instructors.html

VLSI DESIGN VERIFICATION-LAB

(USE ANY EDA TOOL)

LIST OF EXPERIMENTS

1. Design and Verification of Ripple Carry Adder
   (Dataflow, Structural, Gate level, Behavioral, Test bench creation)
2. Implement CRC-4 Encoder using HDL Code
   (Dataflow, Structural, Gate level, Behavioral, Test bench creation)
3. Timing Verification of Ripple Carry Adder
4. Gate level analysis of different stuck at faults in a CMOS Gate.(NAND, NOR)
5. Fault analysis for a given logic circuit.
6. Design of a LFSR and calculate the different power dissipation for the circuit (8bit, 16bit, 32 bit) using BIST
7. Perform timing analysis for a given sequential circuit
Course Outcomes:

At the end of the course the student should be able to:

2. Design networks involving arithmetic operations using VHDL coding.
3. Analyze and design standard combinational modules and Get an insight to the specification, organization and Implementation of RTL systems.
4. Understand data and control subsystems and able to design it.
5. Analyze the specifications and implement a microcomputer system and Learn to design a RTL system for the specifications mentioned.

UNIT-I
10 Hrs

UNIT -II
DESIGN OF NETWORKS FOR ARITHMETIC OPERATIONS: Design of a Serial Adder with Accumulator, State Graph for Control Network, Design of a Binary Multiplier, Multiplication of a Signed Binary Number, and Design of a Binary Divider with VHDL Codes.  
08 Hrs

UNIT-III
STANDARD COMBINATIONAL MODULES: binary decoder, binary encoder, multiplexers and demultiplexers.
12 Hrs
UNIT-IV

10 Hrs

UNIT-V
SPECIFICATION AND IMPLEMENTATION OF A MICROCOMPUTER: Basic component of a micro system, memory subsystem, I/O subsystem, Processors, Operation of the computer and cycle time.

12 Hrs

Reference Books:

HIGH SPEED VLSI DESIGN

Course Code 17VDE112
Hrs./Week 4+0+0+0
Total Hrs. 52

CIE Marks 50
SEE Marks 50
Credits 4

Course Outcomes:

At the end of the course the student will be able to

1. Understand Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures

2. Design Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

3. Know basic Latch design, Latching single-ended logic and Latching Differential Logic.


5. Understand timing issues & clock generation.

UNIT-I
Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic 10 Hrs

UNIT-II
Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise. 12 Hrs

UNIT-III
Latching Strategies, Basic Latch Design, and Latching single-ended logic, Latching Differential Logic. 10 Hrs

UNIT-IV
Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.

Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection. 10 Hrs
UNIT-V
Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques, Skew Tolerant Design 10 Hrs

Reference Books:

SoC DESIGN

Course Code  17VDE113  CIE Marks  50
Hrs./ week  4+0+0+0  SEE Marks  50
Total Hrs.  52  Credits  4

At the end of the course the student should be able to:
1. Understand the benefits and criteria for the design of SoC
2. Understand the architecture, types of processors and memories used in embedded systems.
3. Explain the use of hardware accelerators in a SoC and features of DMA and USB controllers.
4. Explain the different NoC topologies and components in a SoC
5. Explain the SoC design flow

UNIT-I

12 Hrs

UNIT-II
Embedded Processors - microprocessors, microcontrollers, DSP and their selection criteria. Review of RISC and CISC instruction sets, Von-Neumann and Harward architectures, and interrupt architectures.
Embedded Memories - scratchpad memories, cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence.

10 Hrs

UNIT-III
Hardware Accelerators in an SoC - comparison on hardware accelerators and general-purpose CPU. Accelerators for graphics and image processing.

Typical peripherals in an SoC - DMA controller, USB controller.

10 Hrs

UNIT-IV

Mixed Signal and RF components in an SoC - Sensors, Amplifiers, Data Converters, Power management circuits, RF transmitter and receiver circuits.

10 Hrs

UNIT-V
SoC Design Flow - IP design, verification and integration, hardware-software codesign, power management problems, and packaging related problems.

10 Hrs
Reference Books:
ASIC DESIGN

Course Code 17VDE114
Hrs./ week 4+0+0+0
Total Hrs. 52

CIE Marks 50
SEE Marks 50
Credits 4

Course outcomes:
At the end of the course the student should be able to:

1. Describe the concepts of ASIC design methodology, data path elements, operators, I/O cells.
2. Apply logical effort technique for predicting delay, delay minimization and FPGA architectures.
3. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
4. Explain algorithms for floorplanning and placement of cells for optimized area and speed.
5. Explain and apply routing algorithms for optimization of length and speed.

UNIT-I
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.
CMOS Logic: Datapath Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells.

10 Hrs

UNIT-II
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages.
Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.

10 Hrs

UNIT-III
Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.
Low-level design entry: Schematic entry: Hierarchical design, Netlist screener.
Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

12 Hrs

UNIT-IV
Floor planning Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.
Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.

10 Hrs
UNIT-V


10 Hrs

**Reference Books:**

ELECTIVE-II

ADVANCED DIGITAL SYSTEM DESIGN

Course Code 17VDE 121
Hrs./Week 4+0+0+0
Total Hrs. 52
CIE Marks 50
SEE Marks 50
Credits 4

Course outcomes:
At the end of the course the student should be able to:

1. Define Finite State Model. Design Simplified Synchronous State Machines by evaluating equivalent states.
2. Analyze and Design Asynchronous State Machines Identify the different Hazards and design Hazard free circuits.
3. Define different Fault classes and models Design Fault tests using different techniques.
4. Explain the architecture of RAM, ROM, and FPGAs. Design Digital circuits using Programmable Logic
5. Represent and design Digital Circuits in RTL. Define various elements of ASM Charts and design circuits using ASM

UNIT-I


UNIT-II


UNIT-III


UNIT-IV


UNIT-V

Reference Books:

DSP ALGORITHMS & ARCHITECTURE

Course Code 17VDE122
Hrs./Week 4+0+0+0
Total Hrs. 52

CIE Marks 50
SEE Marks 50
Credits 4

Course outcomes:
At the end of the course the student should be able to:

1. Choose DSP core for generic DSP applications.
2. Understand transformation and filter structure for the required analysis.
3. Understand array processing in DSP applications.
4. Apply DSP algorithm for audio, video and multimedia related system development.
5. Understand different compression techniques in the field of signal processing.

UNIT-I
Introduction to Generic DSP’s, Performance and Structural limitations. Measures and Structures for enhancing performance. 12 Hrs

UNIT-II
Filter structures, Transform structures, Data Flow and Control flow issues. 10 Hrs

UNIT-III
Introduction to Array processing, Array processing approaches to DSP solutions. 10 Hrs

UNIT-IV
Some modern DSP algorithms (audio, video and multimedia) and development of new computational and arithmetic building blocks. 10 Hrs

UNIT-V
Architecture development for some Compression and Coding Algorithms. Reference to some standards and development of Architecture based implementation of these. 10 Hrs
Reference Books:

SOFT COMPUTING

Course Code  16VDE123
Hrs./Week    4+0+0+0
Total Hrs.   52
CIE Marks    50
SEE Marks    50
Credits      4

Course Outcomes:

At the end of the course the student should be able to:

1. Answer the situations of real-life such as uncertainty, impression, approximation, partial truth, etc. using nature driven approaches.
2. Develop fuzzy models to solve the wide ranges of uncertainty.
3. Relate and apply global and local optimization methods.
4. Create artificial neural network model in decision support systems.
5. Design computer-aided systems for pattern recognition.

UNIT-I


10 Hrs

UNIT-II


12 Hrs

UNIT-III


10 Hrs

UNIT-IV

NEURAL NETWORKS: Introduction to Neural Network, Adaptive Networks – Feed forward Networks, back propagation algorithm, Self Organizing Maps (SOMs).

10 Hrs
UNIT-V


Reference Books:

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

**Course Code**: 17VDE124  
**CIE Marks**: 50  
**Hrs./Week**: 4+0+0+0  
**SEE Marks**: 50  
**Total Hrs.**: 52  
**Credits**: 4

**Course Outcomes:**

At the end of the course the student should be able to:

1. Explain types of microelectronic designs, levels of abstraction and synthesis process and general approaches to optimization.
2. Analyze graph optimization problems and optimization of graphs, logic minimization using Boolean algebra.
3. Apply HDLs synthesis optimization techniques, HDL compiler optimizations, architectural level synthesis and optimization techniques for data path and control path.
4. Explain and apply logic minimization algorithms and techniques, optimization principles for two level combinational logic.
5. Apply state based model and network based model for sequential circuit optimization, algorithms for area optimal library binding.

**UNIT-I**

**Introduction**: Microelectronics, semiconductor technologies and circuit taxonomy, Microelectronic design styles, computer aided synthesis and optimization

**Graphs**: Notation, undirected graphs, directed graphs, combinatorial optimization, Algorithms, tractable and intractable problems, algorithms for linear and integer programs, graph optimization problems and algorithms, Boolean algebra and Applications.  

**UNIT-II**

**Hardware Modeling**: Hardware Modeling Languages, distinctive features, structural hardware language, Behavioral hardware language, HDLs used in synthesis, abstract models, structures logic networks, state diagrams, data flow and sequencing graphs, compilation and optimization techniques.

**Schedule Algorithms**: A model for scheduling problems, Scheduling with resource and without resource constraints, Scheduling algorithms for extended sequencing models, Scheduling Pipe lined circuits.
UNIT-III

Two level combinational logic optimization: Logic optimization, principles, operation on two level logic covers, algorithms for logic minimization, symbolic minimization and encoding property, minimization of Boolean relations. 10 Hrs

UNIT-IV

Multiple level combinational optimizations: Models and transformations for combinational networks, algebraic model, Synthesis of testable network, algorithm for delay evaluation and optimization, rule based system for logic optimization. 10 Hrs

UNIT-V

Sequential circuit optimization: Sequential circuit optimization using state based models, sequential circuit optimization using network models.

Cell library binding: Problem formulation and analysis, algorithms for library binding, specific problems and algorithms for library binding (lookup table F.P.G.As and Antifuse based F.P.G.As), rule based library binding. 12 Hrs

Reference Books:

ADVANCES IN VLSI DESIGN

Course Code: 17VDE201
Credits: 5

Hours/Week: 4+0+0+1
CIE: 50 Marks

Total Hours: 52
SEE: 50 Marks

Course Outcomes:

At the end of the course the student should be able to:

1. Select a suitable semi-custom design approach to design a desired digital system and analyze the MISFET, MOSFET and MODFETs in equilibrium and under bias.
2. Understand the need for super buffers to drive large capacitive loads and analyze the energy band diagrams of MISFETs under different bias.
3. Apprehend the short channel effects and design pass-transistor circuit for given logic.
4. Analyze the effect of scaling, understand the challenges to CMOS technology and revolutionary advances beyond CMOS.
5. Design barrel shifter, tally circuit, CMOS multiplexers and apply routing algorithms to determine minimum length path for interconnects.

UNIT I

Review of MOS Circuits: MOS and CMOS static plots, CMOS switches

System Design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, programmable structure, standard cell approach, Full custom Design, Gate arrays, Programmable inter connect

MESFET and MODFETs: Structure, operations, quantitative description of MESFETS.

UNIT II

MIS Structures and MOSFETS: MIS systems in equilibrium, under bias, small signal operation of MESFETS and small signal analysis of MOSFETS.

Super Buffers: NMOS super buffers, NMOS tri-state super buffer and pad drivers, CMOS super buffers, RC delay lines

UNIT III

Short Channel Effects: Two dimensional Potential profile, High electric field in the short channel, Punch-through and channel length modulation.

Steering Logic: Driving large capacitive loads, pass-transistor logic, designing pass-transistor logic, Dynamic ratio less inverters, General functional blocks - NMOS and CMOS functional blocks.
UNIT -IV

Scaling Theory: Constant filed, constant voltage and quasi-constant voltage models

Beyond CMOS: Evolutionary advances beyond CMOS: SOI MOSFET 4 Hrs

Revolutionary advances beyond CMOS: carbon Nano-tubes, Conventional vs. tactile computing, molecular and biological computing.

Moleciontrols-Molecular Diode and diode- diode logic 5 Hrs

Defect tolerant computing.

Challenges to CMOS: Processing Challenges to Further CMOS Miniaturization.

UNIT-V

Special Circuit Layouts and Technology Mapping: Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logics, NMOS, CMOS Multiplexers, Barrel shifter. 7 Hrs

Wire routing Algorithms: Need for algorithms, study of Lee-Moore Maze running algorithm and line search algorithm. 5 Hrs

Reference Books:


ADVANCES IN VLSI DESIGN LAB

(Use any of the EDA Tools)

List of Experiments

1. Design and simulation to implement hierarchy and regularity in a design: Develop Verilog code and perform simulation using testbench for:

   . Adder

   . Transmission Gate based multiplexer

   . Synchronous and asynchronous counters

2. Design and simulation Pass-Transistor logic (PT logic) for various logic functions.
3. Schematic simulation of a given logic function using:
   . NAND-NAND logic
   . NOR-NOR logic
   . AOI logic


5. Design and simulation of a barrel shifter.
DESIGN OF ANALOG VLSI CIRCUITS

Course Code: 17VDE202
Hrs./Week: 4+0+2+0
SEE Marks: 50
CIE Marks: 50
Total Hrs.: 52
Credits: 5

Course Outcomes:

At the end of the course the student should be able to:

1. Explain MOSFET operation, characteristics, second order effects and device models
2. Design and analyze single stage amplifiers using MOSFETs.
3. Design and analyze differential amplifiers using MOSFETs and current mirrors.
4. Analyze the high frequency behavior and noise in analog circuits using MOSFETs
5. Design and analyze operational amplifiers using MOSFETs, Implement oscillators, VCO and PLL in CMOS technology.

UNIT-I
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models. MOS Device as a Capacitor 8 Hrs

UNIT-II
Single stage Amplifier: CS stage with resistance load, diode connected load, current source load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascode stage, Folded cascode, choice of device models. 10 Hrs

UNIT-III
Differential Amplifiers: Basic difference pair, common mode response, Differential pair with MOS loads, Gilbert cell.
Passive and active Current mirrors: Basic current mirrors, Cascode current mirrors, active current mirrors. 12 Hrs

UNIT-IV
Frequency response of Amplifier: General considerations. Common source stage, source follower, Common gate stage, Cascode stage and Difference pair. Noise in CS stage, CG stage, source follower, cascode stage, differential pair. 12 Hrs

UNIT-V
Operational Amplifiers: One Stage OP-Amp, Two Stage OP-Amp, Gain boosting, Common Mode Feedback, Slew rate, PSRR. Compensation of two stage OP-Amp, Other compensation techniques.
Oscillators: Ring Oscillators, LC Oscillators, VCO, Mathematical Model of VCO.
PLL: Simple PLL, Charge pump PLL, Non-ideal effects in PLL, Delay locked loops and applications. 10 Hrs
Reference Books:


ANALOG & MIXED MODE VLSI LAB

LAB EXPERIMENTS:

Tool to be used: CADANCE/SYNOPSIS/MENTOR GRAPHICS.

1. Design a single stage amplifier using MOSFETs for the given specifications.
2. Design a differential amplifier using MOSFETs for the given specifications.
3. Design a two stage op-amp for the given specification. Determine the frequency response, slew rate, offset effects and Noise.
4. Design a simple sample and hold circuit and measure the switching times.

Design flow:

1. Draw the schematic and verify the following
2. DC Analysis
3. AC Analysis
4. Transient Analysis
5. Draw the Layout and verify the DRC, ERC
6. Check for LVS
REAL TIME OPERATING SYSTEMS

Course Code 17VDE203
Hrs./Week 4+0+2+0
Total Hrs. 52

CIE Marks 50
SEE Marks 50
Credits 5

Course Outcomes:

After studying this subject, the student should be able to:

1. Know the history of real-time operating systems, and acquire knowledge on basic concepts of RTOS such as utility, scheduling and its theories, RTOS characteristics etc.
2. Examine the operational principle of different scheduling algorithms and their characteristics.
3. Analyze concepts related to I/O and Memory resources, examine basic problems faced by multi-resource services, and solve challenges faced by soft real time services.
4. Recognize and resolve software and hardware challenges faced by real-time system to meet service deadlines, and get awareness on embedded system components and debugging components.
5. Analyze basic performance tuning procedures to design better systems, and explore high reliability and high availability designs.

Unit-I


12 Hrs

Unit-II


10 Hrs

Unit-III

Memory: Physical Hierarchy, Capacity and Allocation, Shared Memory, ECC Memory: Illustration using Hamming encoding, Flash Fill Systems.


Soft-Real-Time Services: Missed Deadlines, Quality of Service, Alternatives to Rate Monotonic Policy, Mixed Hard and Soft Real-Time Services. 10 Hrs

Unit-IV


Debugging Components: Exceptions, Asserts, Checking Return Codes, Single-Step Debugging, Test Access Ports, Trace Ports, Power-On Self-Test and Diagnostics, Application Level Debugging. 10 Hrs

Unit-V

Performance Tuning: Basic Concepts of Drill-Down Tuning, Hardware-Supported Profiling and Tracing, Building Performance Monitoring into Software, Path Length, Efficiency, and Call Frequency, Fundamental Optimizations.


Design of RTOS: PIC Microcontroller.

Case Studies Based on MUCOS, VxWorks such as ACVM, Sending Application Layer Byte Streams on TCP/IP Stack, and Smart Card Application. 10 Hrs

Reference Books:

Real Time Operating Systems LAB

Program List

Use RT-LINUX/SOLARIS/QNX Operating System ONLY.

1. Write a program for Thread Creation and Termination.
2. Create independent threads each of which will execute some function and wait till threads are complete before main continues. Unless we wait run the risk of executing an exit which will terminate the process and all threads before the threads have completed.
3. Create the N number of threads and find the how many threads are executed.
4. Create threads numbers 1-3 and 8-10 as permitted by functionCount1 and create threads number 4-7 as permitted by functionCount2 and print final count value.
5. Design and execute a program using any thread library to create the number of thread specified by the user, each thread independently generates a random integer as an upper limit and then computes and prints the number of primes less than or equal to that upper limit, along with that upper limit.
6. Rewrite above program (Program 5) such that the processes instead of thread are created and the number of child processes created is fixed as two. The program should make use of kernel timer to measure and print the real time, processor time, User space time and kernel space time for each process.
7. Design develop and implement a process with a producer thread and a consumer thread which make use of a bounded buffer (Size can be prefixed at suitable value) for communication. Use any suitable synchronization construct.
8. Design develop and execute a program to solve a system of n liner equations using successive over-relaxation method and n processes which use shared memory API.
ELECTIVE-III

ADVANCED COMPUTER ARCHITECTURE

Course Code 17VDE211
Hrs./Week 4+0+0+0
Total Hrs. 52

CIE Marks 50
SEE Marks 50
Credits 5

Course Outcomes:

At the end of the course the student should be able to:

1. Analyze the fundamental issues in architecture design and their impact on application performance.
2. Understand advanced issues in design of computer processors, caches, and memory.
3. Analyze performance trade-offs in computer design.
4. Apply knowledge of processor design to improve performance in algorithms and software systems.
5. Acquire experience with tools for statistical analysis of instruction set trade-offs.

UNIT – I

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multifactor and SIMD computers.
Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms.

10 Hrs

UNIT – II

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

10 Hrs

UNIT – III


10 HRS

UNIT – IV

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

10 Hrs
UNIT - V

**Multiprocessor architectures:** Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, and MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, and synchronization. Scalable point -point interfaces: Alpha364 and HT protocols, high performance signaling layer. Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine checks, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.

12 Hrs

**REFERENCE BOOKS:**

R2. Hwan and Briggs, "Computer Architecture and Parallel Processing", MGH.VLSI  

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ALGORITHMS FOR VLSI

Course Code        17VDE212                     CIE Marks    50
Hrs./Week          4+0+0+0                       SEE Mark     50
Total Hrs.         52                              Credits      4

Course outcomes:
At the end of the course the student should be able to:
1. Explain and apply graph minimization algorithms.
2. Write code for algorithms used for computational and geometrical simplification and minimization using
data structures for CAD tools.
3. Explain and write code for partitioning, floorplanning, chip planning and pin assignment.
4. Explain different algorithms used for placement of cells during the physical design of a chip.
5. Explain and write code for algorithms used for routing of cells, clock and power supply.

UNIT-I
Graph Algorithms: Graph search Algorithms, Spanning tree Algorithm, Shortest path Algorithm, Matching
Algorithm, Min cut and Max cut Algorithms and Steiner Tree Algorithm. 10 Hrs

UNIT-II
Computational geometry Algorithms: Line sweep method and extended line sweep method.

Basic data structures: Linked list of blocks, Bin based method, neighbor pointers and corner stitching.

Graph Algorithms for physical design: Classes of graphs in physical design, relationship between graph classes,
graph problems, Algorithms for interval graphs and Algorithms for permutations graphs. 10 Hrs

UNIT-III
Partitioning: Group migration Algorithms.

Floor planning and Pin assignment: floor planning, chip planning and pin assignment. 10 Hrs

UNIT-IV
Placement: Simulated annealing, simulated evolutions, force directed placement, sequence pair technique,
Breuer’s Algorithm, Terminal propagation Algorithm, Cluster growth and quadratic assignment. 10 Hrs
UNIT-V


Over the cell routing, Via minimization, clock, power and ground routing.  

12 Hrs

Reference books:


LOW POWER VLSI DESIGN

Course Code           17VDE213
Hrs./Week             4+0+0+0
Total Hrs.            52

CIE Marks            50
SEE Marks            50
Credits              4

Course outcomes:
At the end of the course the student should be able to:

1. Analyze the different types of power dissipation in VLSI Circuits
2. Understand the different techniques of power estimation and analysis
3. Understand the different approaches of Low power design at circuit level
4. Understanding the different low power architecture and systems
5. Understand the different approaches of low power clock distribution and algorithm and architectural level methodologies

UNIT-I
Introduction : Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches, Physics of power dissipation in CMOS devices.
Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

12 Hrs

UNIT-II
Power estimation, Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Data Correlation Analysis in DSP Systems, Monte Carlo simulation.
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

10 Hrs

UNIT-III
Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

10 Hrs
UNIT-IV

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

10 Hrs

UNIT-V

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network.


10 Hrs

Reference Books:
NANOTECHNOLOGY

Course Code  17VDE214
Hrs./Week    4+0+0+0
Total Hrs.   52

CIE Marks  50
SEE Marks  50
Credits    4

Course outcomes:
At the end of the course the student should be able to:

1. Understand the broad overview of Nano technology, material, manufacturing and applications in the field of renewable energy.
2. Understand the growth of zero dimensional nano-structures
3. Understand the growth of one dimensional nano-structures
4. Understand the growth of two dimensional nano-structures
5. Understand the thin film fundamentals and transport phenomena

Unit-I

Introduction  Overview of nano-technology

Materials and manufacture  Nanoengineering of polymer bio-medical devices, nano-powder production, nanomaterial technology, nanotechnology devices, nanoparticles manufacture, analytical methods for nanotechnology.

Nanotechnology for renewable energy  Energy intensity of materials, hydrogen energy, battery technology, nanotechnology alternative to existing batteries, fuel cell technology, power generation using nanotechnology, solar energy and nano technology, wind power and nanotechnology.  

Unit-II

ZERO DIMENSIONAL NANO-STRUCTURES  Nano particles through homogenous nucleation; Growth of nuclei, synthesis of metallic nano particles, Nano particles through heterogeneous nucleation; Fundamentals of heterogeneous nucleation and synthesis of nano particles using micro emulsions and Aerosol.

Unit-III

Unit-IV

**Two Dimensional nano-structures**: Fundamentals of film growth. Physical vapour Deposition (PVD): Evaporation molecular beam epitaxy (MBE), Sputtering, Comparison of Evaporation and sputtering. Chemical Vapour Deposition (CVD): Typical chemical reactions, Reaction kinetics, transport phenomena, CVD methods, diamond films by CVD.

10 Hrs

Unit-V

**Thin Films** Atomic layer deposition (ALD), Electrochemical deposition (ECD), Sol-Gel films, Advantages, Disadvantages and Applications of thin films

**Transport Phenomena** Confinement and Transport in nanostructure, Current, Reservoirs and Electron channels, Conductance formula for nanostructures,Quantized conductance. Local density of states. Ballistic transport, Coulomb blockade, Diffusive transport.

10 Hrs

**References:**


ELECTIVE-IV

SYSTEM DESIGN USING EMBEDDED PROCESSORS

Course Code: 17VDE221  
Hrs./Week: 4+0+0+0  
Total Hrs.: 52  
CIE Marks: 50  
See Marks: 50  
Credits: 4

Course Outcomes:

At the end of the course the student should be able to:

1. Learn the architecture, instruction set and program the 8051 microcontroller.
2. Understand the architecture, programming model and memory organization of 32-bit ARM920T processor.
3. Learn ARM, Thumb instruction set and the interrupt handling of ARM920T processor.
4. Understand the architecture and peripherals of ARM9 microcontroller.
5. Be familiar with development & debugging tools for microcontroller based embedded systems.

UNIT-I

8-Bit Microcontrollers:

Architecture: CPU Block diagram, Memory Organization, Program memory, Data Memory, Interrupts
Peripheral: Timers, Serial Port, I/O Port
Programming: Addressing Modes, Instruction Set, Programming

Microcontroller based System Design: A typical application design from requirement analysis through concept design, detailed hardware and software design using 8-bit 8051 Microcontrollers.  

12 Hrs

UNIT-II

32-Bit ARM920T Processor Core:

Introduction: RISC/ARM Design Philosophy, About the ARM920T Core, Processor Functional Block Diagram
Programmers Model: Data Types, Processor modes, Registers, General Purpose Registers, Program Status Register, CP15 Coprocessor, Memory and memory mapped I/O, Pipeline, Exceptions, Interrupts and Vector table, Architecture revisions, ARM Processor Families.

Memory Management Units: How virtual memory works, Details of the ARM MMU, Page Tables, Translation Look-aside Buffer Domains and Memory access permissions  

10 Hrs
UNIT-III

**ARM Instruction Set:** Data Processing instructions, Branch instructions, Load - Store instructions, Software Interrupt Instruction, Program Status Register Instruction, Loading Constants

**Thumb Instruction Set:** Thumb register usage, ARM-Thumb interworking, Branch instruction,

Data processing instructions, Load - store instructions, stack instructions, software interrupt instructions.

**Interrupt Handling:** Interrupts, Assigning interrupts, Interrupt latency, IRQ & FIQ exceptions, Basic interrupt stack design, and implementation, Non-nested Interrupt handler.

10 Hrs

UNIT-IV

**ARM9 Microcontroller Architecture:**

AT91RM9200 Architecture: Block Diagram, Features, Memory Mapping

**Memory Controller (MC):** Memory Controller Block Diagram, Address Decoder, External Memory Areas, Internal Memory Mapping.

**Parallel Input/output Controller (PIO).**

**Interrupt Controller:** Normal Interrupt, Fast Interrupt, AIC.

**System Timer (ST):** Period Interval Timer (PIT), Watchdog Timer (WDT), Real-time Timer (RTT), Real Time Clock (RTC)

10 Hrs

UNIT-V

**Development & Debugging Tools for Microcontroller based Embedded Systems:**

Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc.

10 Hrs

Reference Books:


MEMS AND IC INTEGRATION

Course Code: 17VDE222
CIE Marks: 50
Hrs./Week: 4+0+0+0
SEE Marks: 50
Total Hrs.: 52
Credits: 4

Course Outcomes:

At the end of the course the student should be able to:

1. Understand CMOS IC Fabrication
2. Understand the MEMS Design methodology
3. Understand various Mechanical Sensors and its applications
4. Understand various Electronics Sensors and its applications
5. Understand the scaling issues in MEMS

UNIT-I
Overview of CMOS process in IC fabrication – Crystal growth, doping, Growth and deposition of dielectric layers, epitaxial growth, masking and photolithography, etching, metallization, surface and bulk micromachining, LIGA process, wafer bonding.

UNIT-II
MEMS system-level design methodology, Equivalent Circuit representation of MEMS, signal-conditioning circuits, and sensor noise calculation.

UNIT-III
Pressure sensors with embedded electronics (Analog/Mixed signal), Accelerometer with transducer, Gyroscope, Bolo meter

UNIT-IV
RF MEMS, Optical MEMS

UNIT-V
MEMS scaling issues

Reference Books:

VLSI SIGNAL PROCESSING

Course Code   17VDE223
Hrs./ week  4+0+0+0
CIE Marks  50
SEE Marks  50
Total Hrs.   52
Credits  4

Course Outcomes:

At the end of the course the student will be able to

1. Explain pipelining, parallel processing & data flow representation.
2. Understand retiming, unfolding, algorithmic strength reduction in filters.
3. Know fast convolution, systolic architecture.
4. Understand digital lattice filter structures, bit level arithmetic architecture.
5. Know low power design, programmable digital signal processors & their applications.

UNIT-I

Introduction to DSP systems – Data flow representations - Iteration Bound – Pipelined and parallel processing.  12 Hrs

UNIT-II

Retiming – unfolding – algorithmic strength reduction in filters and transforms.  10 Hrs

UNIT-III

Systolic architecture design – fast convolution – pipelined and parallel recursive and adaptive filters.  10 Hrs

UNIT-IV

Scaling and round off noise – digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic.  10 Hrs

UNIT-V

Numerical strength reduction – synchronous, wave and asynchronous pipelines – low power design – programmable digit signal processors & applications.  10 Hrs
Reference Books:

CMOS RF CIRCUIT DESIGN

Course Code  17VDE224  
CIE Marks  50  
Hrs./ week  4+0+0+0  
SEE Marks  50  
Total Hrs.   52  
Credits   4

Course Outcomes:

At the end of the course the student should be able to:

1. Understand the basic concepts of RF design and behavior of passive components
2. Realize the behavior of BJT and MOSFET parameters at RF range
3. Apply the Smith chart and design high frequency amplifiers
4. Explain the biasing and referencing in devices at RF range and identify different kinds of noise
5. Design RF circuits and explain RF synthesizers.

UNIT-I

Introduction to RF design and Wireless Technology:

Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion, characteristics of passive IC components, resistor, capacitor and inductor.

10 Hrs

UNIT-II

BJT and MOSFET Behavior at RF Frequencies:


10 Hrs

UNIT-III

The Smith chart:  S – parameters.

High-frequency Amplifier Design: Zeros as bandwidth enhancers, Shunt-series amplifier, Bandwidth enhancement with fT doublers, Tuned amplifiers, Neutralization and unilateralization, Cascaded amplifiers.

10 Hrs

UNIT-IV
Voltage Reference and Biasing:
Review of diode behavior, Diodes and Bipolar Transistors in CMOS technology, Supply-independent bias circuits, Band gap voltage reference, Constant-gm bias.

UNIT-V
RF Circuits Design:
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, various mixers-working and implementation.
Oscillators -Basic topologies VCO and definition of phase noise, Noise power and trade off.
Radio frequency Synthesizers - PLLS, Various RF synthesizer architectures and frequency dividers,
Design issues in integrated RF filters.

Reference Books:
LabVIEW Basics

Course Code AP006  CIE Marks  50
Hrs./ week 2+0+0+0  SEE Marks  50
Total Hrs. 26  Credits  Nil

Syllabus:

1. Introduction to LabVIEW: Front panel, Block diagram, Tool palette, Control palette, Run, stop, and abort.
2. Numerical palette, String palette, Boolean palette and Comparison palette.
3. Case structure, formula structure.
5. The while loop and its applications: Need for time delay; Different ways of connecting the conditional terminal.
6. For Loop: applications and examples to fill array.
7. Use of shift registers for using data from previous iterations, applications.
8. Manipulating strings with examples.
11. Project work.

Evaluation based on Hands-On tasks during the course.